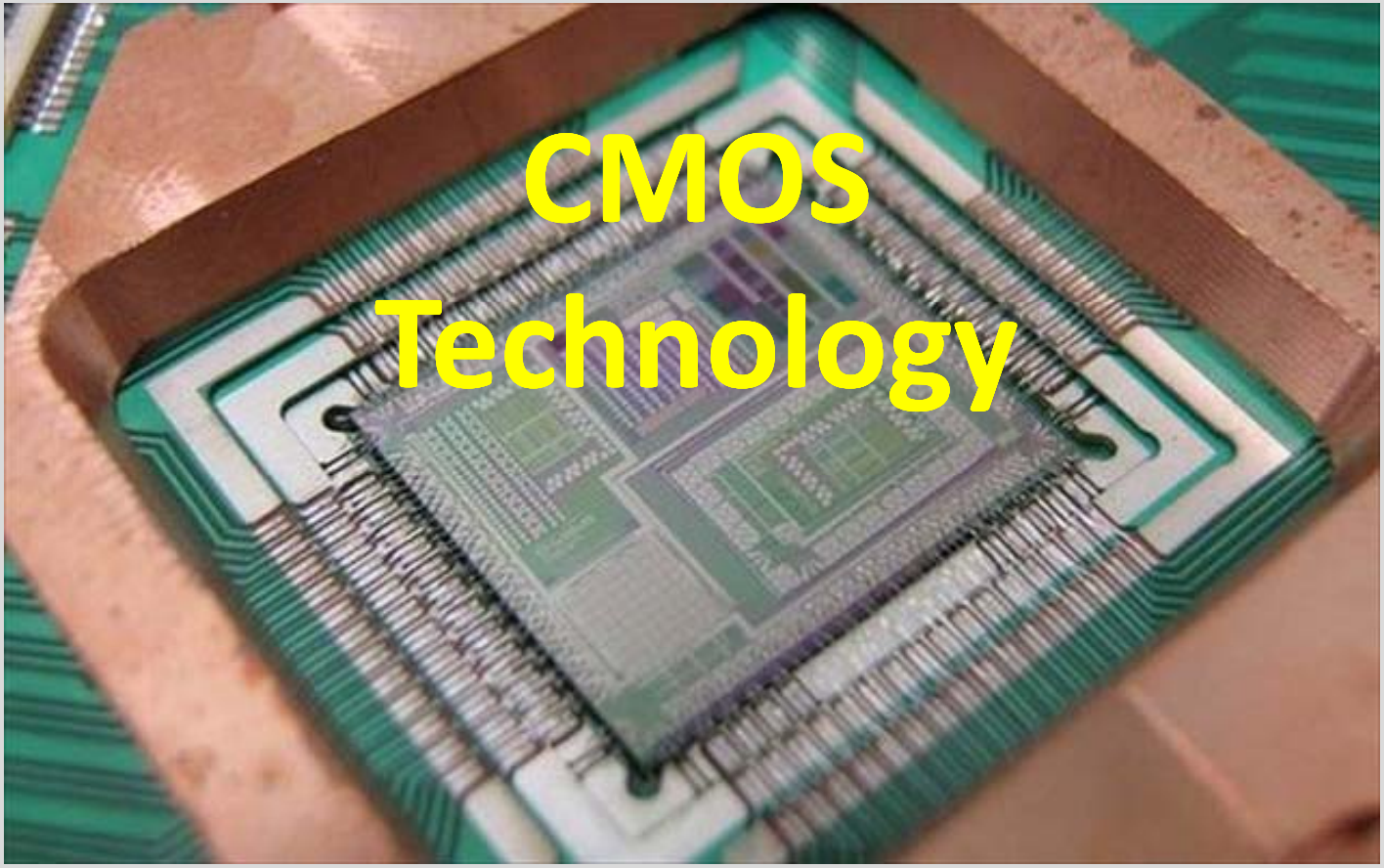
ΚΥΚΛΩΜΑΤΑ VLSI

Πανεπιστήμιο Ιωαννίνων



Τμήμα Μηχανικών Η/Υ και Πληροφορικής

From the book: An Introduction to VLSI Process
By: W. Maly

ΚΥΚΛΩΜΑΤΑ VLSI

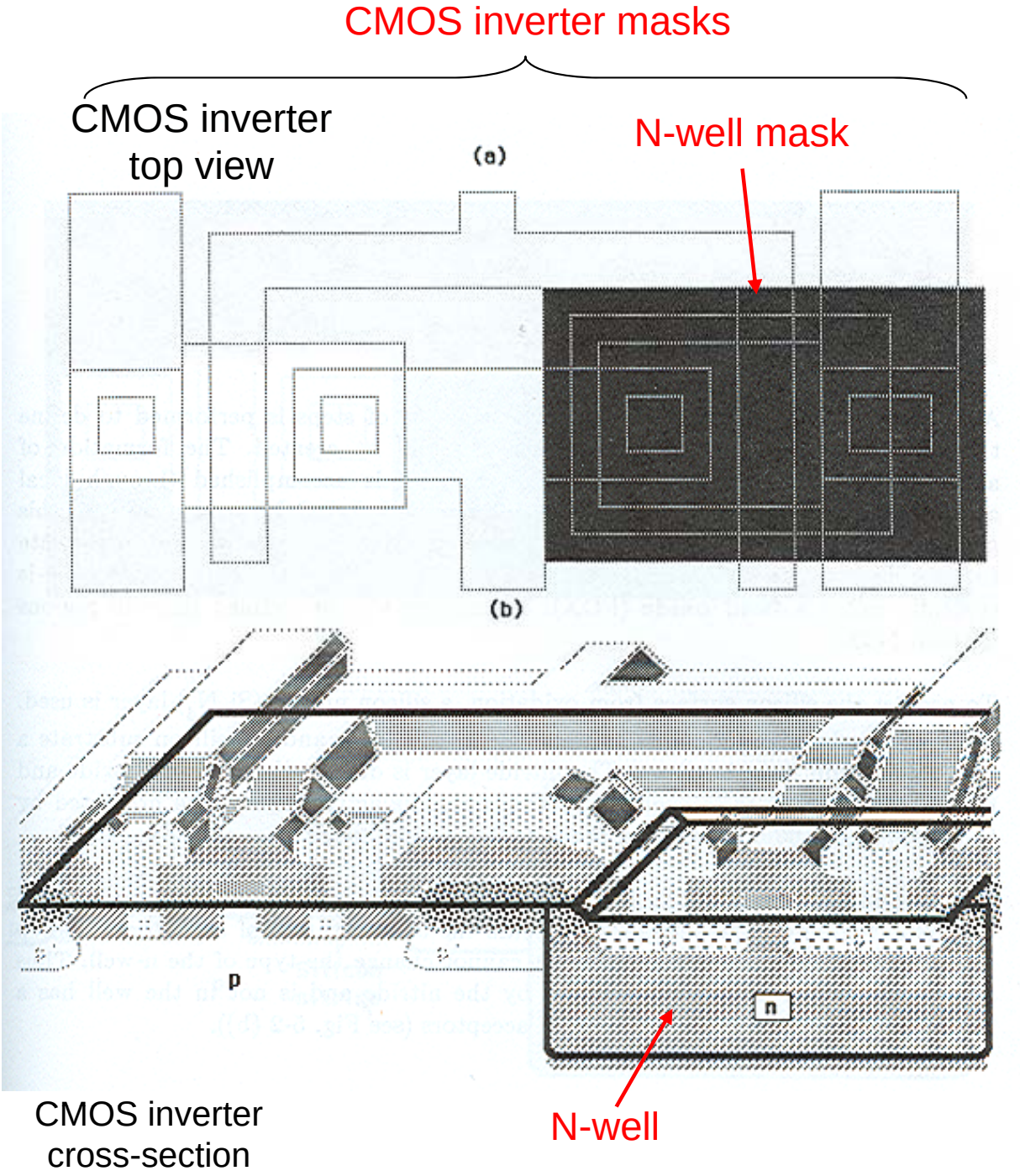
Διάρθρωση

1. N-well CMOS
2. Active region formation
3. Gate oxide growth
4. Polysilicon deposition
5. n-MOS – p-MOS S/D implantation
6. S/D annealing
7. SiO_2 deposition
8. Contact cuts
9. Metal deposition
10. Passivation

VLSI Systems
and Computer Architecture Lab

N-well CMOS

N-well implantation in a p-type substrate.



Active Region Formation

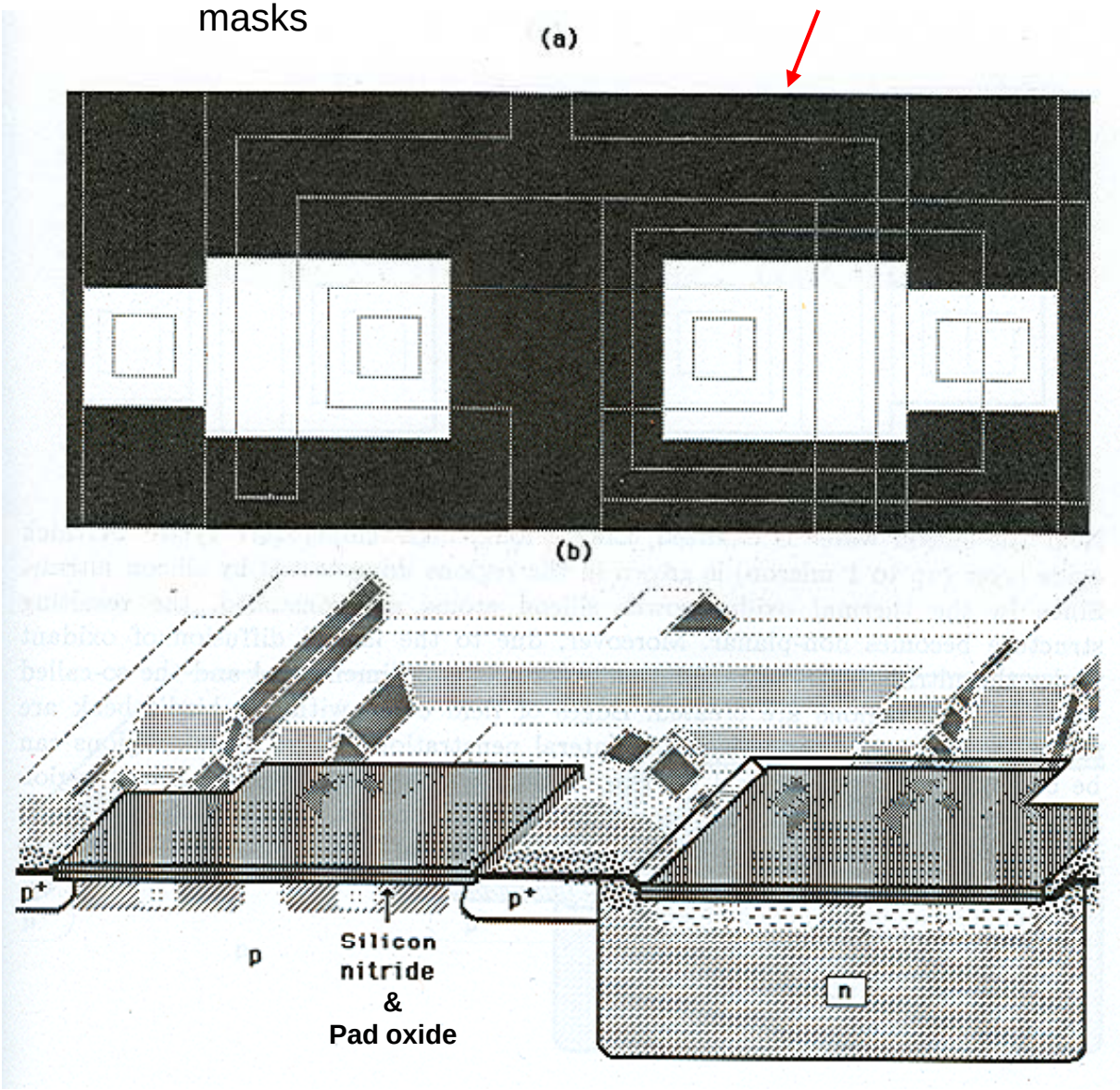
In this process, thick regions of SiO_2 are selectively grown to provide isolation between pMOS and nMOS transistors. This thick oxide is called field oxide (FOX).

The transistors are developed in the regions without FOX that are called active regions.

To protect the transistors' area from oxidation a thin pad oxide layer and a Si_3N_4 layer are used.

CMOS inverter masks

Active mask

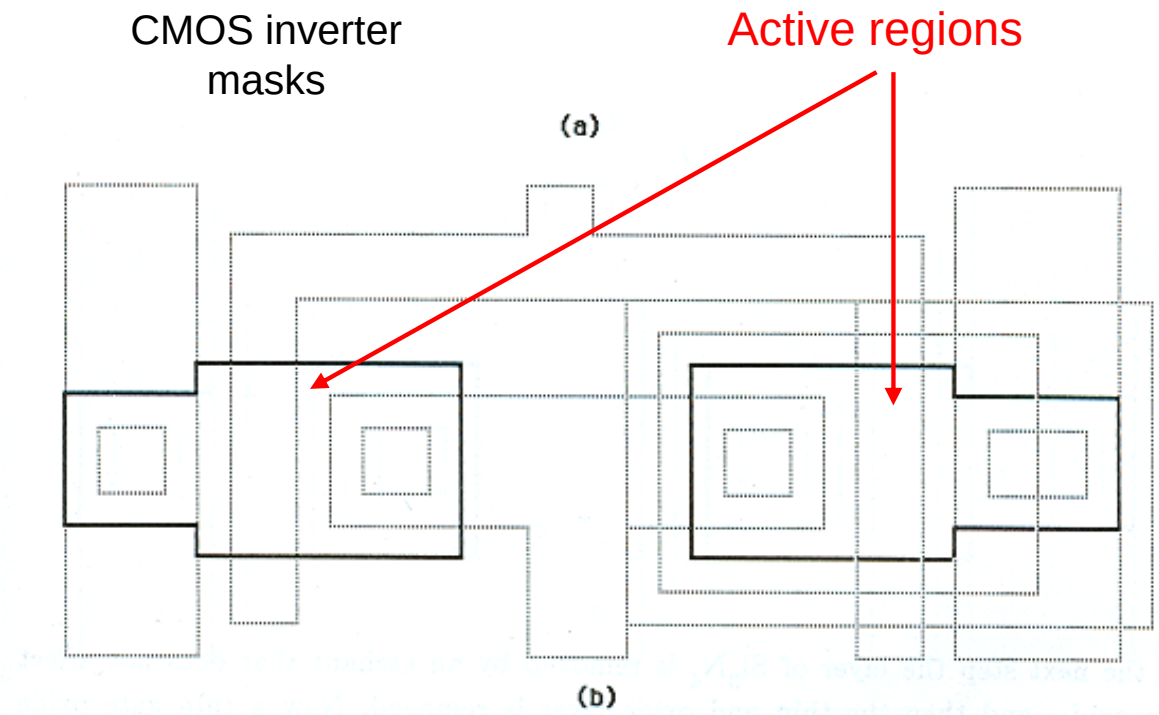


CMOS inverter cross-section

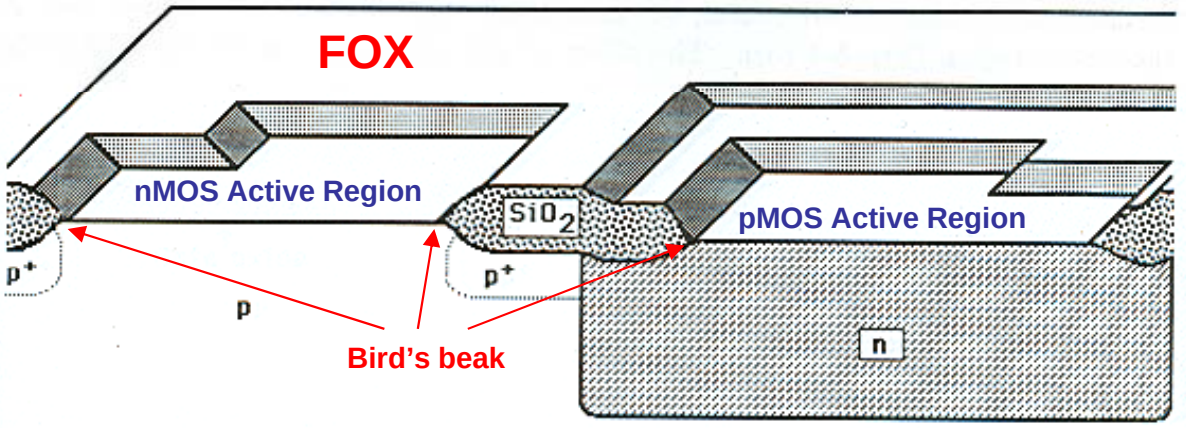
Active Region Formation

Silicon wafer oxidation using a long and high-temperature cycle to develop the thick FOX.

The FOX is grown in the regions unprotected by Si_3N_4 (active regions).



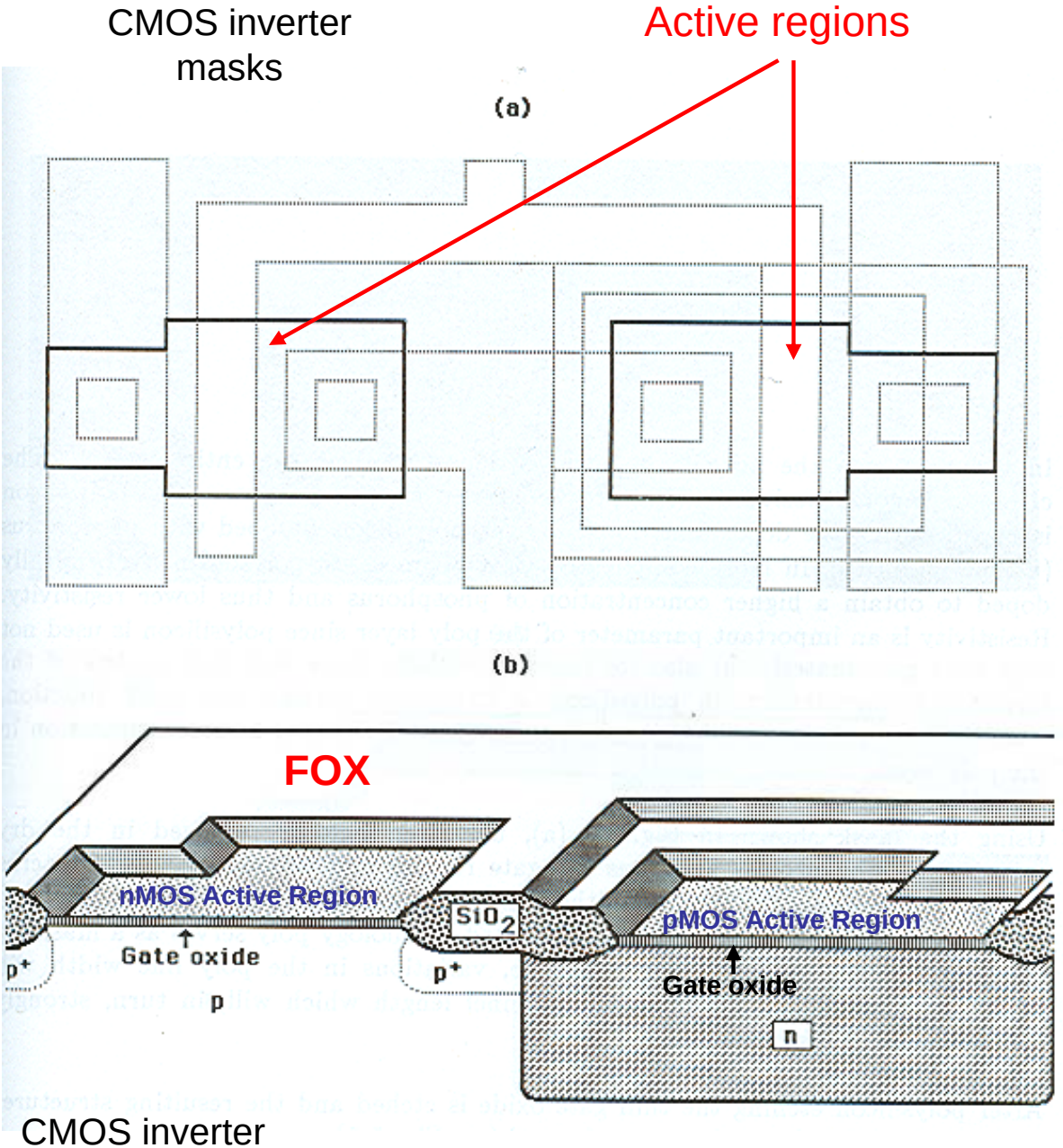
CMOS inverter masks



CMOS inverter cross-section

Gate Oxide Growth

Next the layers of the Si_3N_4 and the pad oxide are removed by an etching process. Then a very thin gate oxide layer is grown thermally in the open area of the active regions.



CMOS inverter cross-section

Polysilicon Deposition

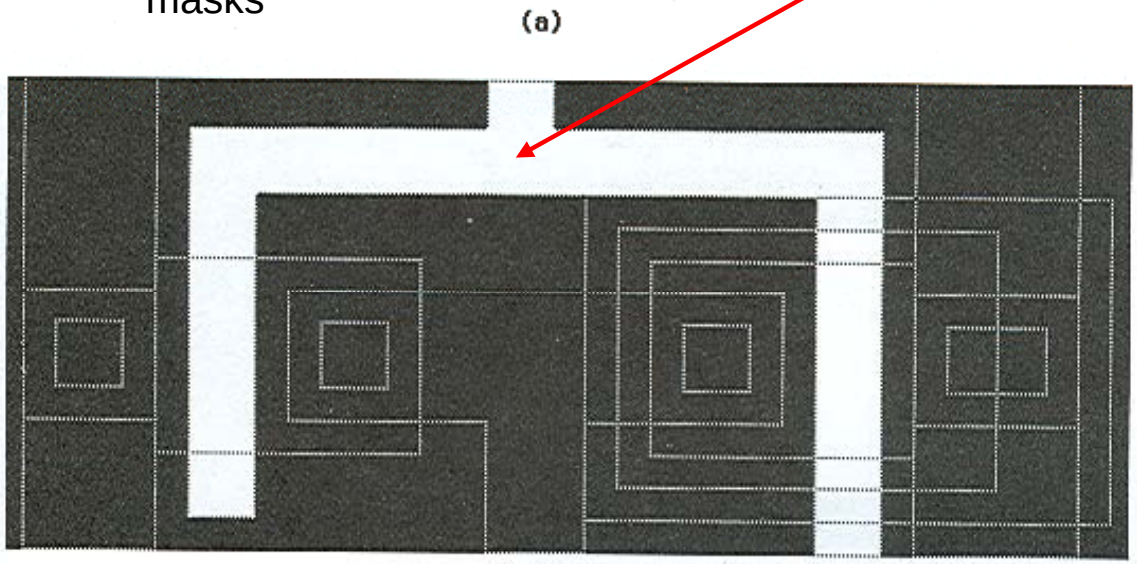
The polysilicon layer is deposited over the entire wafer, using the CVD process.
The poly is doped for reduced resistance.

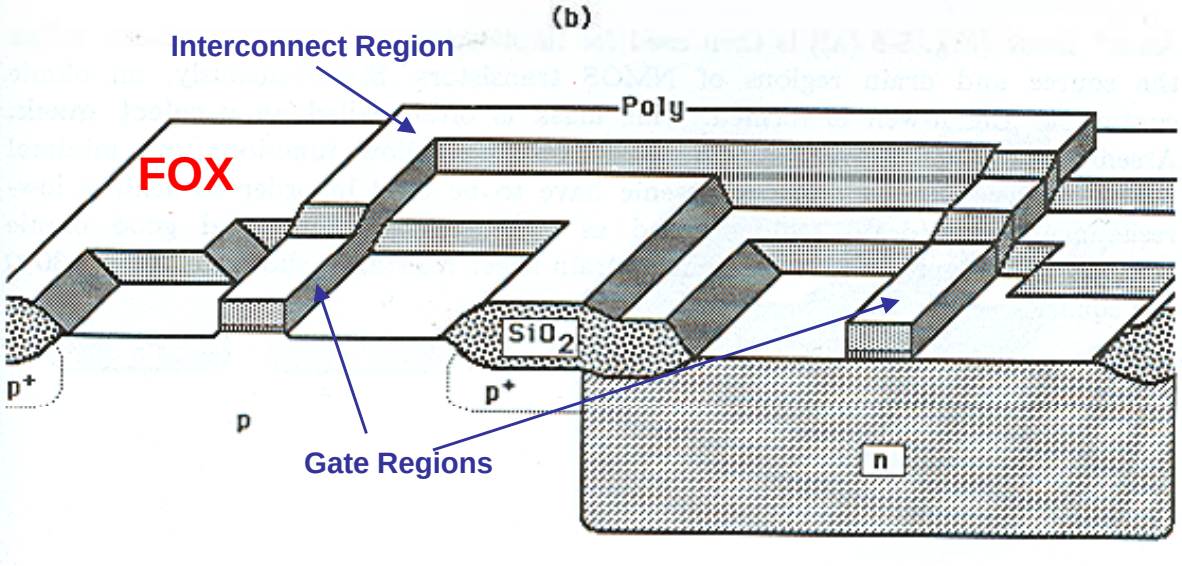
Using the mask in the Fig. the undesired poly is removed by a dry etching process.

The poly serves as a mask for source/drain implantation step (self aligned technology).
After poly etching, the gate thin oxide is also etched.

CMOS inverter masks

Polysilicon region



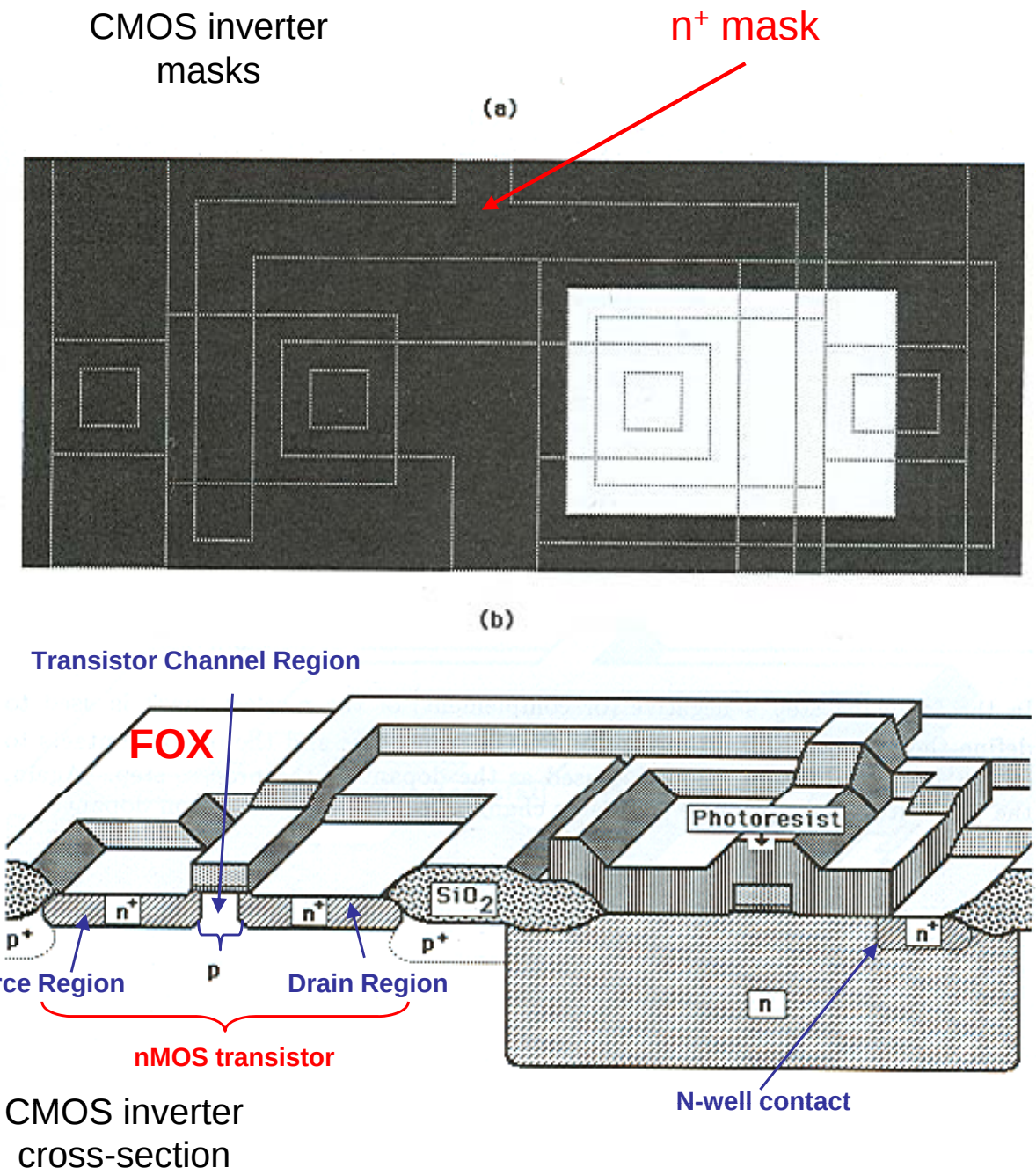


CMOS inverter cross-section

nMOS S/D Implantation

An n^+ mask is used for nMOS source/drain implantation and formation of the bias contact to the N-well.

The polysilicon layer protects the transistor channel region.

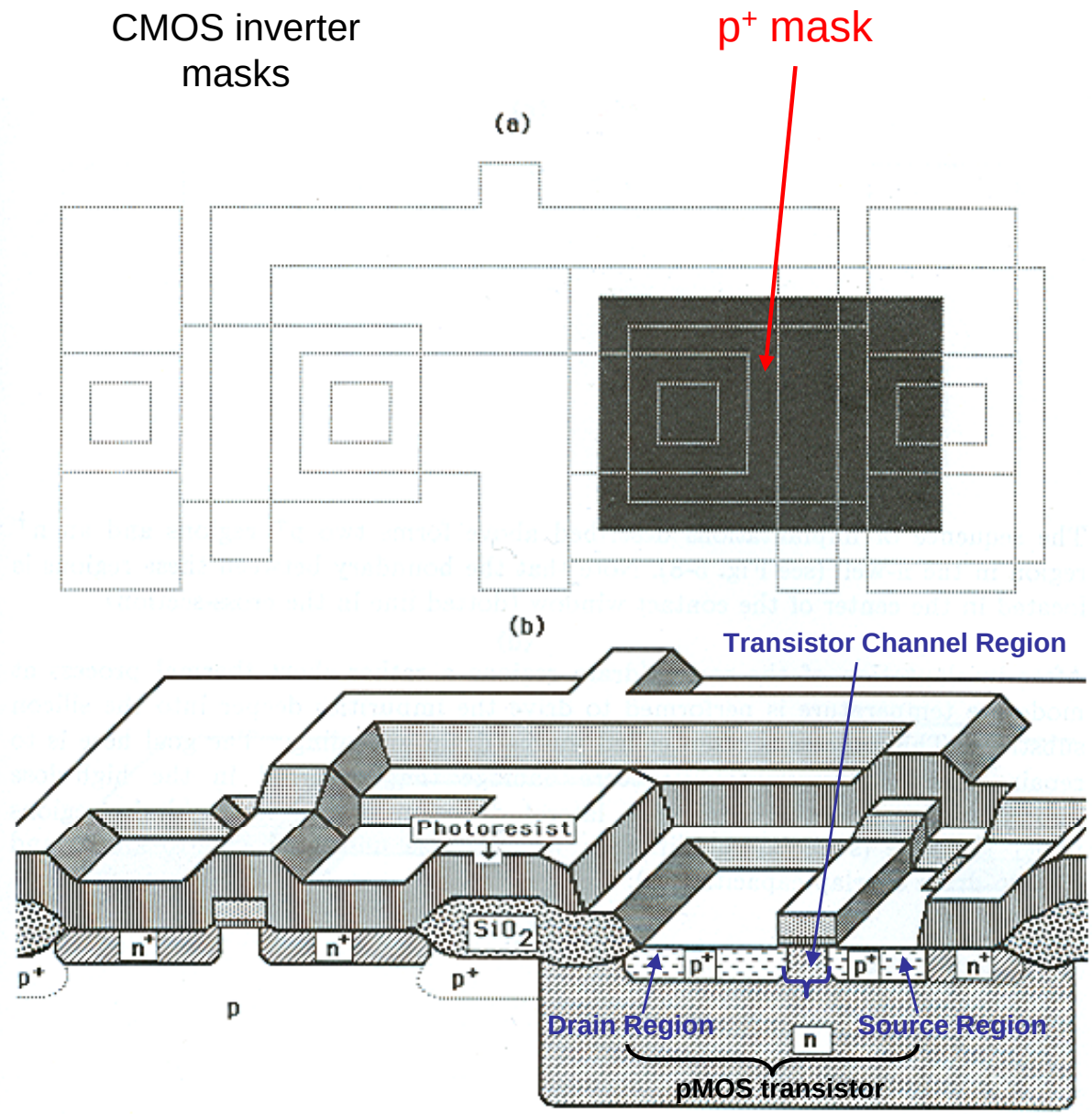


pMOS S/D Implantation

A p^+ mask (negative/complement to the n^+ mask) is used for pMOS source/drain implantation.

Once again, the polysilicon layer protects the transistor channel region.

CMOS inverter masks

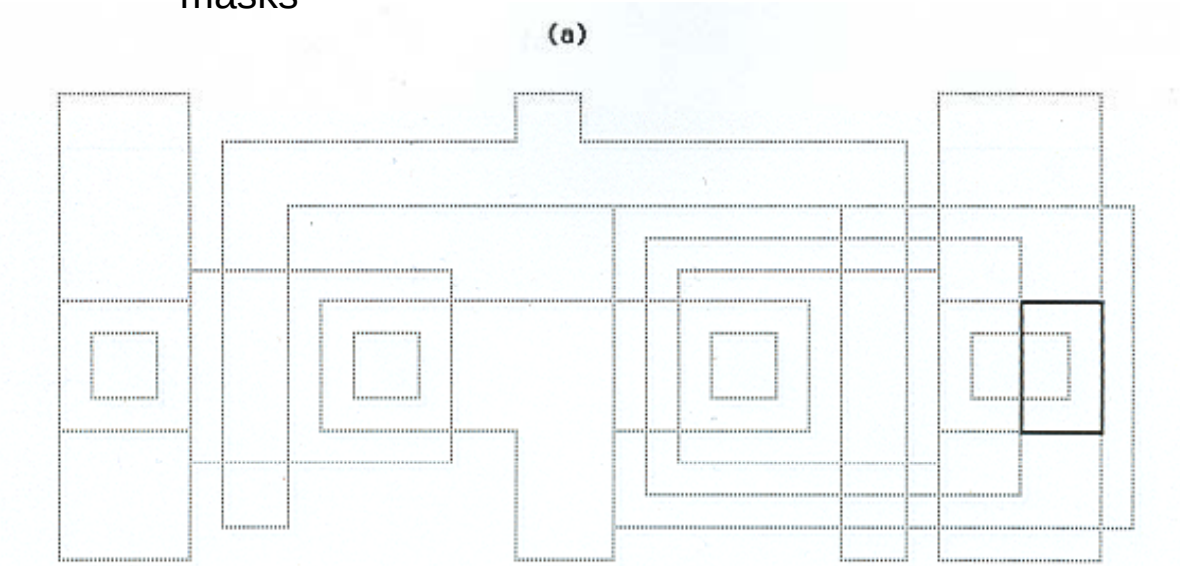


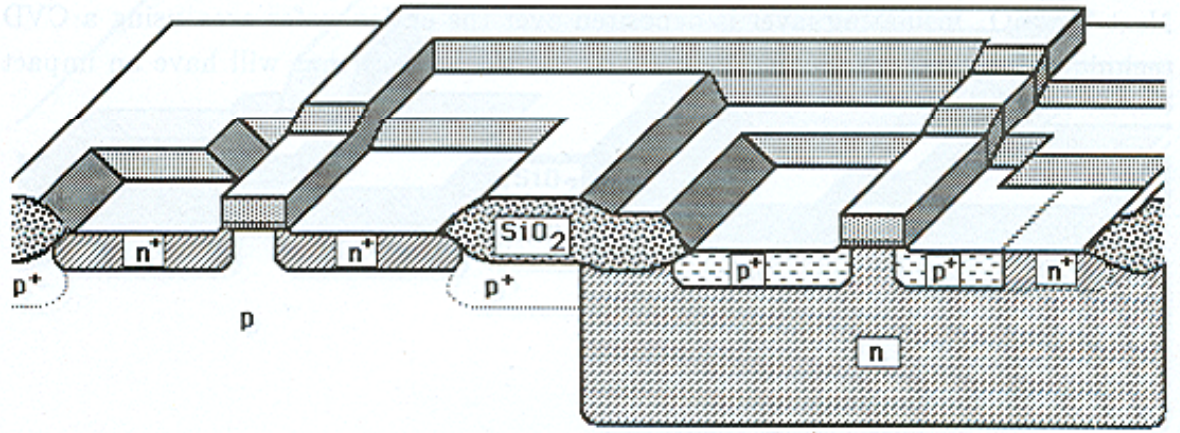
CMOS inverter cross-section

S/D Annealing

After source/drain implantation a short thermal process at moderate temperature is performed.
This way some of the crystal structure damage, occurred in the high-dose implantation, is repaired.

CMOS inverter masks





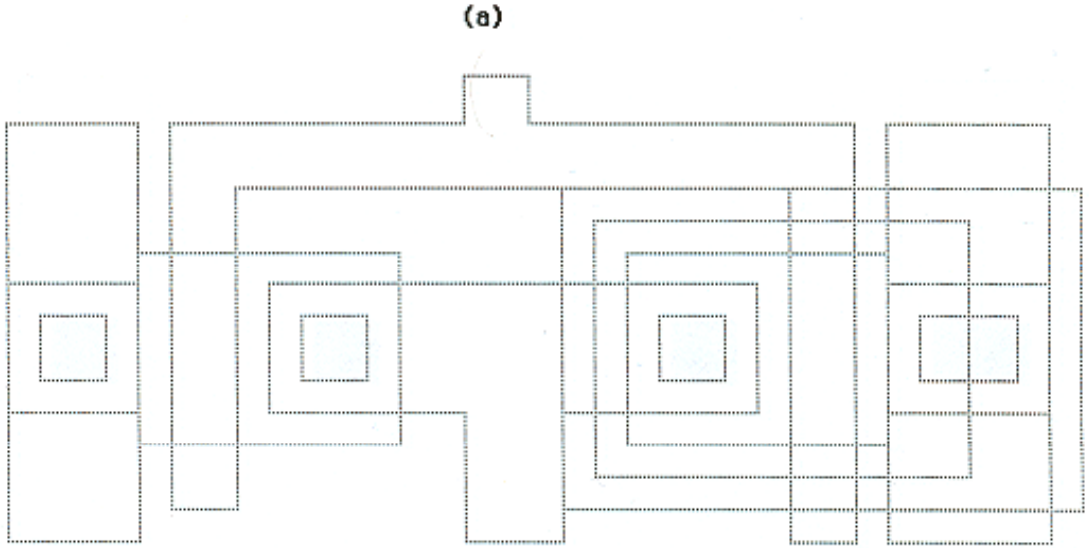
CMOS inverter cross-section

SiO_2 Deposition

The SiO2 insulating layer is deposited over the entire wafer using the CVD technique.

Note the non-planarity of the surface that will have an impact on the metal deposition step.

CMOS inverter masks



CMOS inverter cross-section

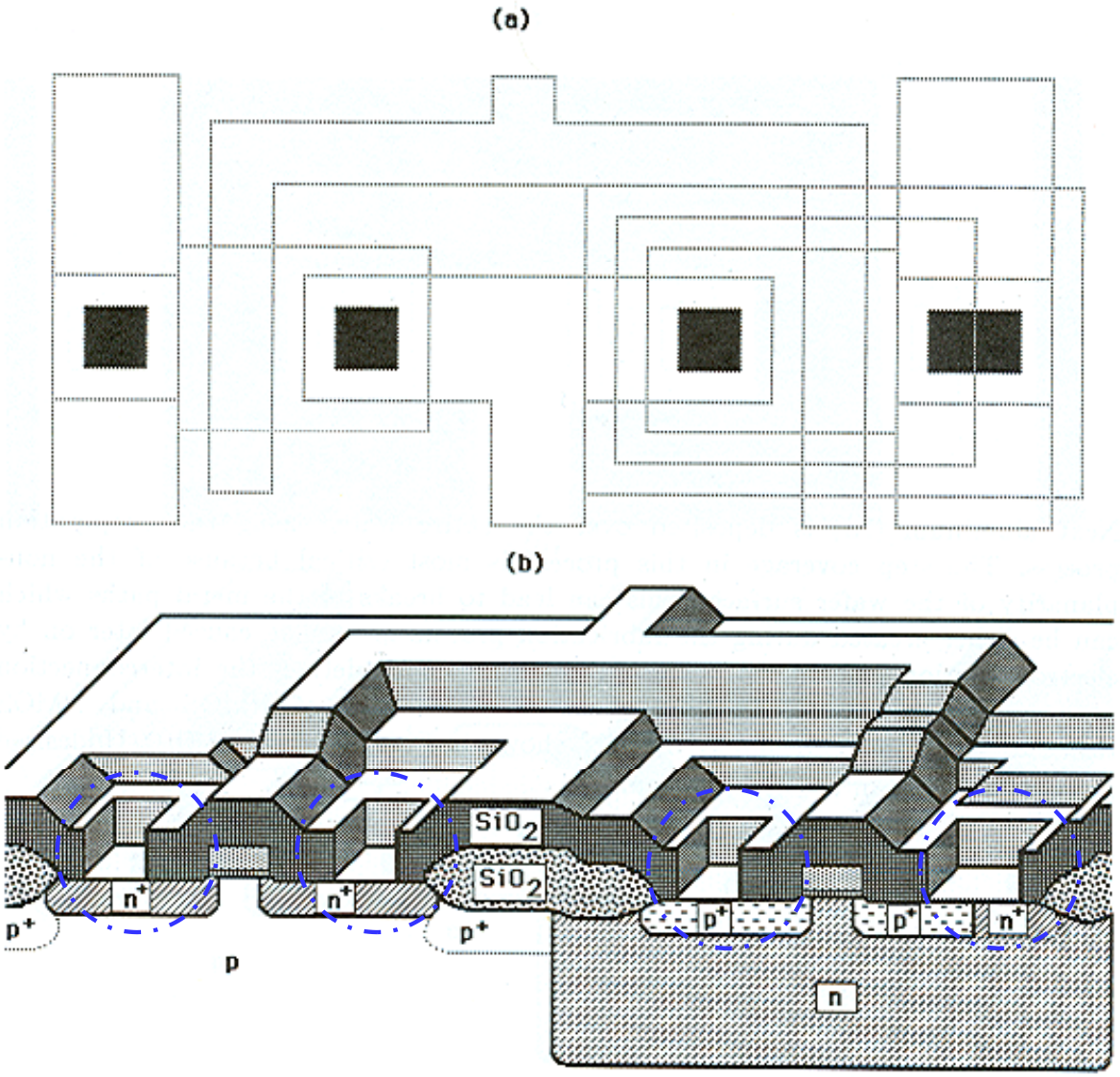
Contact Cuts

A lithographic step to define contact cuts in the insulating layer.

The silicon of the S/D areas is exposed.

The contact cut to the polysilicon layer of the gate is not shown.

CMOS inverter masks



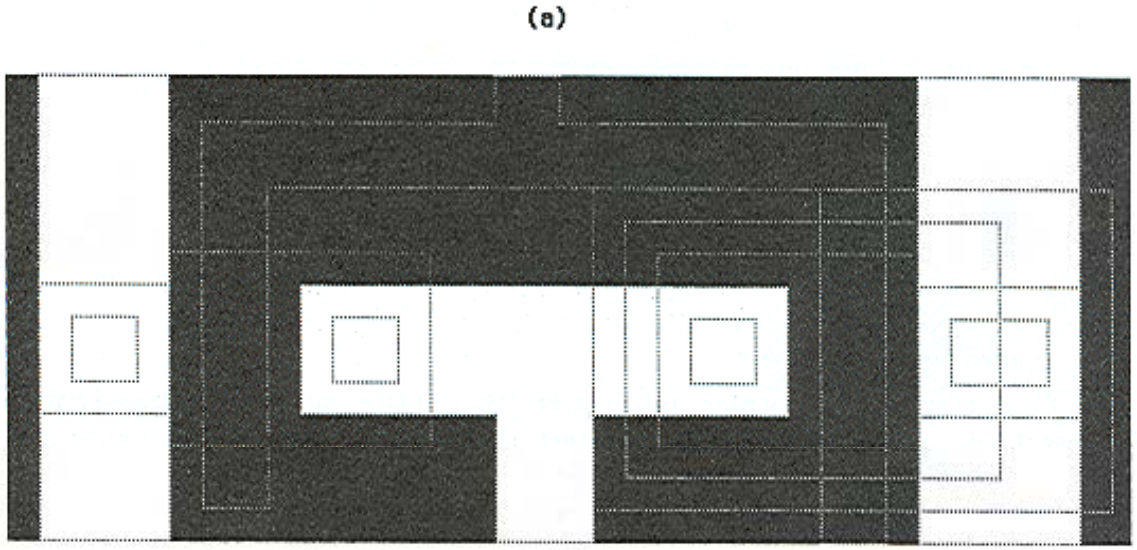
CMOS inverter cross-section

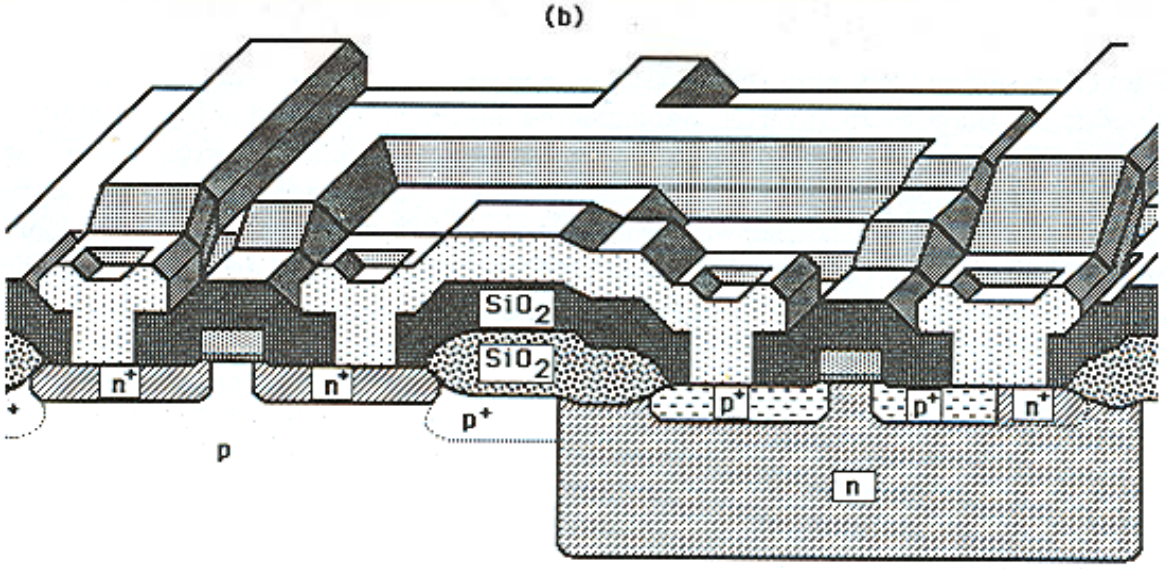
Metal Deposition

The 1st metal layer (Al or Cu) is deposited over the entire wafer using the evaporation process.

The non-planarity of the surface may cause breaks in the metal paths during the fabrication process or later on by electromigration phenomena.

CMOS inverter masks





CMOS inverter cross-section

Passivation

The final step is the passivation (overglass layer) for surface protection
This step is not shown here.

The CMOS inverter, layout (a), cross-section (b) and electrical diagram (schematic) (c), are illustrated in the figure.