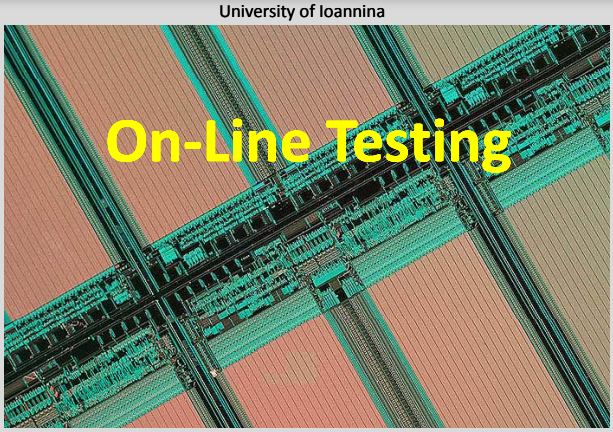
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

University of Ioannina



Dept. of Computer Science and Engineering

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CMOS Integrated Circuit Design Techniques

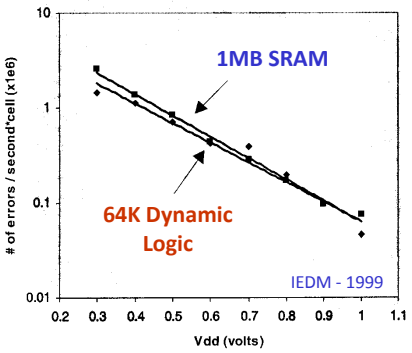
VLSI Systems
and Computer Architecture Lab

Overview

1. ***Reliability issues – Transient faults***
2. ***Soft errors***
3. ***Timing errors***
4. ***Error tolerance design techniques***

Reliability in Nanometer Technologies

Soft Error Rate (SER) increases with technology scaling



SER vs V_{DD}

The evolution (scaling) of CMOS technology results in:

- the reduction of the transistor size
- the increment of the operating frequency
- the reduction of the power supply voltage
- the increment of the transistors' number in a die

which in turn affect the circuit noise margins and reduce their reliability.

Transient Faults and On-Line Testing

- ***Permanent Faults***: faults that permanently affect the circuit operation.
- ***Temporary Faults***: faults that do not affect permanently the circuit operation and are discriminated to:
  - **Transient Faults**: due to random fault generation mechanisms like power supply disturbance, electromagnetic interference, radiation e.t.c.
  - **Intermittent Faults**: due to the degradation of the circuit characteristics.

- **On-Line Testing**: testing procedures are performed during the circuit operation.
  - **Concurrent Testing**: testing is performed concurrently to the circuit normal operation.
  - **Periodic Testing**: testing is performed periodically when the circuit is in the idle mode of operation.
- **Off-Line Testing**: testing is performed when the circuit is not used (e.g. manufacturing testing).

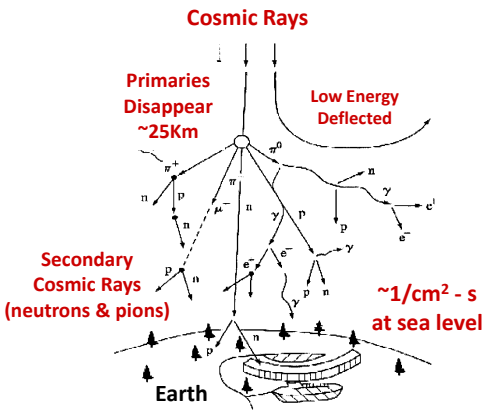
Requirements

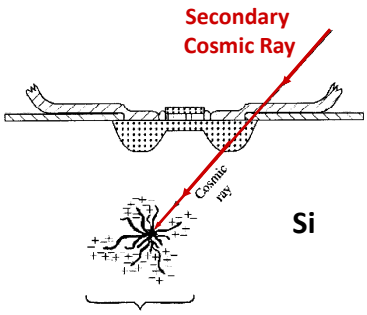
We need design techniques and architectures that will guarantee the correct operation under any circumstances. Techniques that will provide error resiliency or error detection / correction capabilities.
We need self-checking and concurrent testing mechanisms. We need self-healing architectures that will dynamically react to overcome technology and environmental related variabilities and which will be capable to recover after an error generation and will operate correctly even in the presence of failures.

Towards this direction, error tolerance techniques have been proposed:

- error correction codes and self-checking circuits and checkers
- error mitigation techniques aiming to reduce error rates
- error detection and correction methodologies

Radiation and Soft Errors (I)

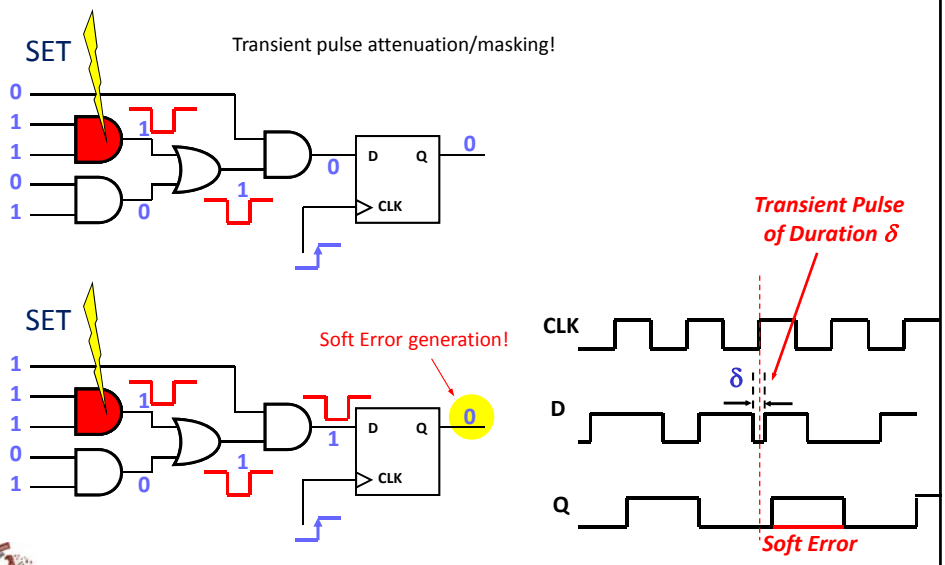




Problem with Soft Errors in VLSI circuits due to Single Event Transients (SETs) and Single Event Upsets (SEUs) generated by:

- emitted α-particles by package impurities
- cosmic ray particles (neutrons, protons and pions)

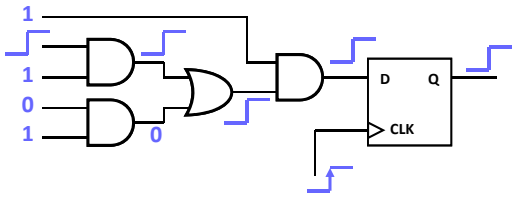
Radiation and Soft Errors (II)



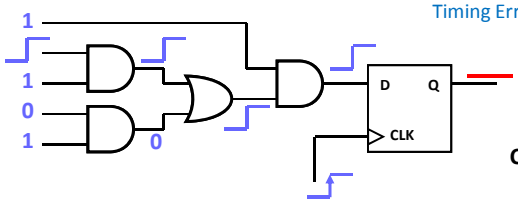
Timing Errors (I)

- Transient faults due to crosstalk, power supply disturbance or ground bounce and environmental variations (e.g. temperature gradients) contribute to timing error generation. Device aging (BTI, HCI effects) is also an important source of timing errors.
- Timing verification turns to be a hard task. Moreover, the increased path delay deviations, due to process variations and the statistical behavior of nano-devices, as well as the manufacturing defects that affect circuit speed may result in timing errors that are not easily detectable (in terms of test cost) in high frequency and high device count ICs. Considering also the huge number of paths in modern circuit designs along with the complexity of testing, it is easy to realize that a significant number of defective ICs may pass the fabrication tests.
- Modern systems running at multiple frequency and voltage levels may suffer from timing errors due to environmental and process related (and also data dependent) variabilities that can affect circuit performance.

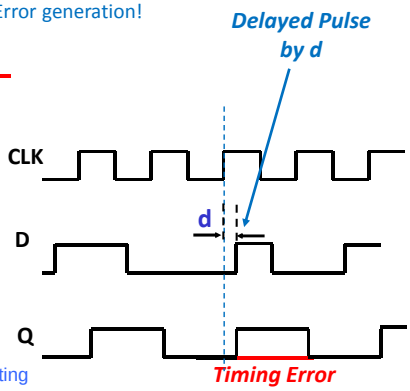
Timing Errors (II)



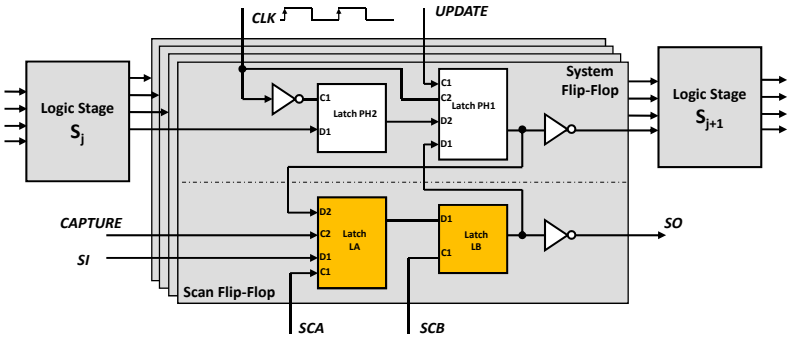
Error free case



Timing Error generation!



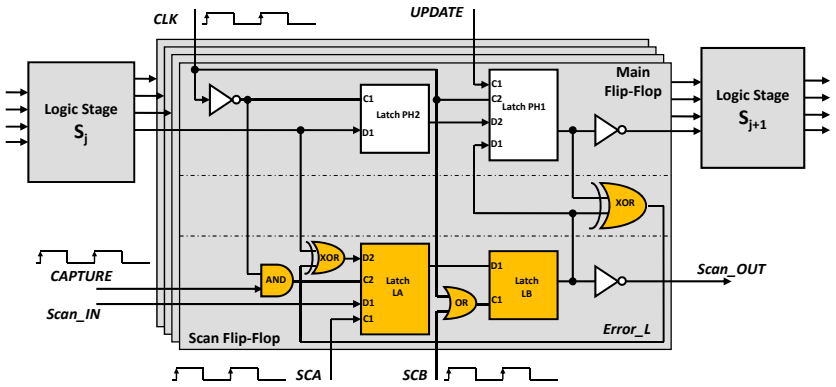
The Scan Design Topology of Intel



Separated System and Scan Flip-Flops

Extra cost of one Flip-Flop

Intel's Error Resilience Approach

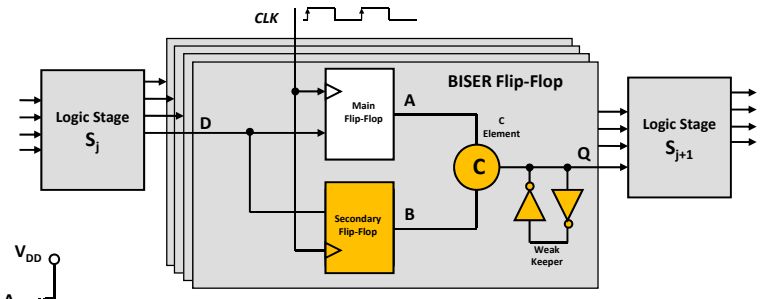


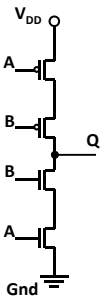
- Additional cost of: 1Flip-Flop, 2 XOR, 1 AND and 1 OR per Flip-Flop !
- The error detection latency is high !

Univ. of Stanford & Intel

IEEE Computer, 38 (2), 2005

The BISER Architecture



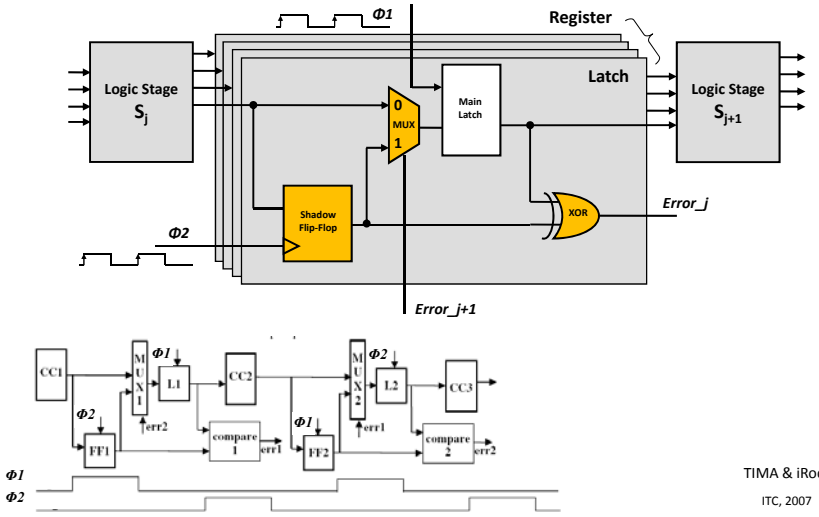


Muller C-Element

Univ. of Stanford & Intel

ICICDT, 2007

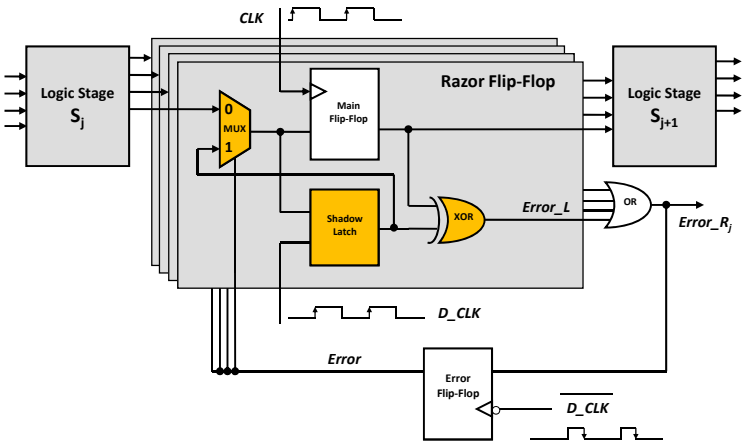
The GRAAL Architecture



TIMA & iRoc

ITC, 2007

The Razor Topology

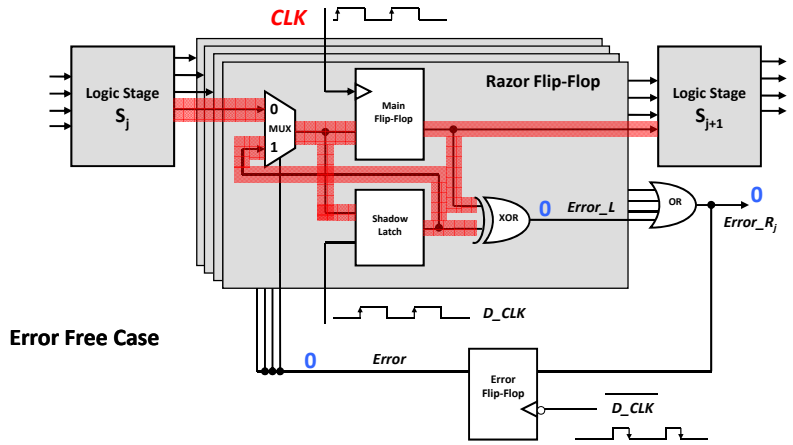


- Additional cost of: 1 Latch, 1 XOR, and 1 MUX per Flip-Flop !

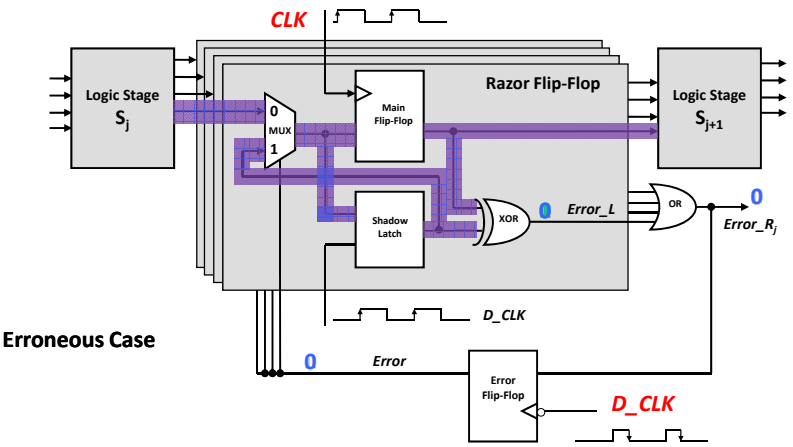
Univ. of Michigan & ARM

IEEE Computer, 37 (3), 2004

The Razor Operation (I)

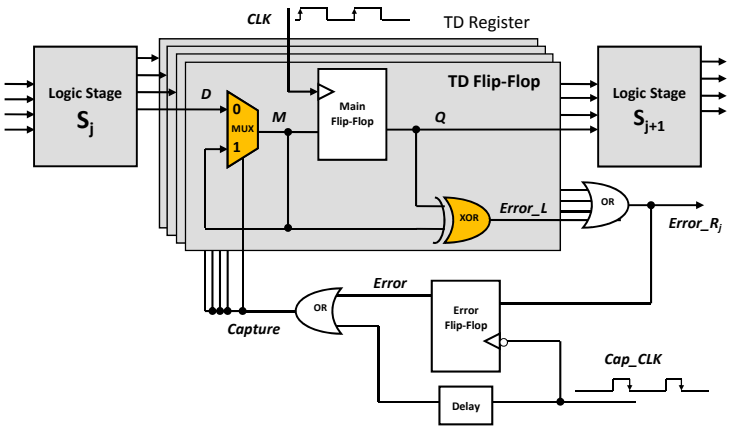


The Razor Operation (II)



- No error detection latency!
- One clock cycle cost for error correction!

The Time Dilation Topology

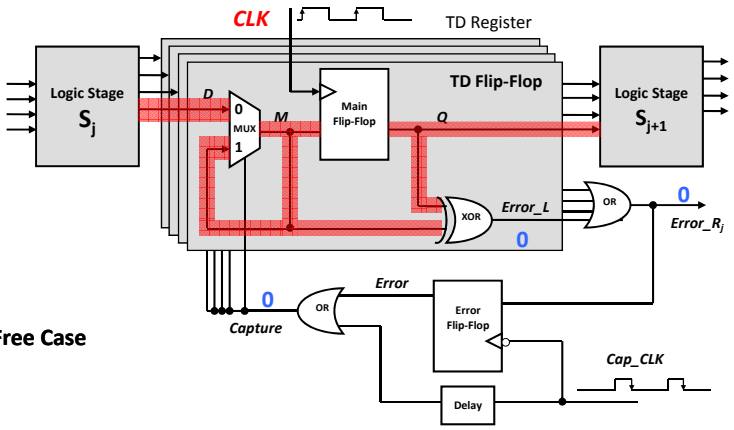


- Additional cost of: 1 XOR, and 1 MUX per Flip-Flop.

Univ. of Ioannina & Athens

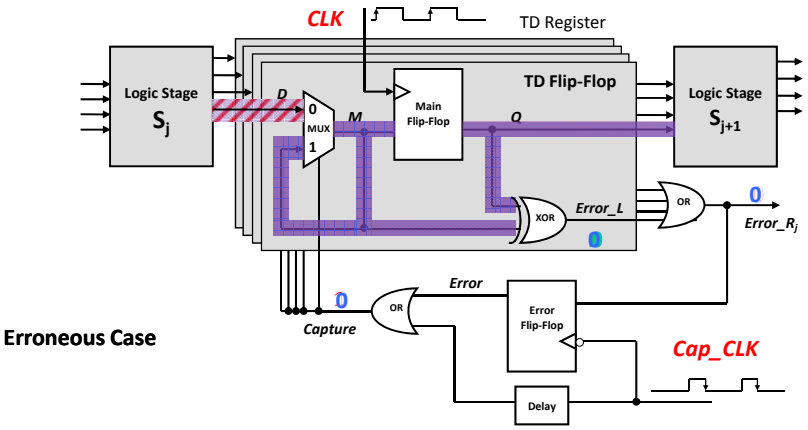
IEEE ICECS, 2006

The Time Dilation Operation (I)



Error Free Case

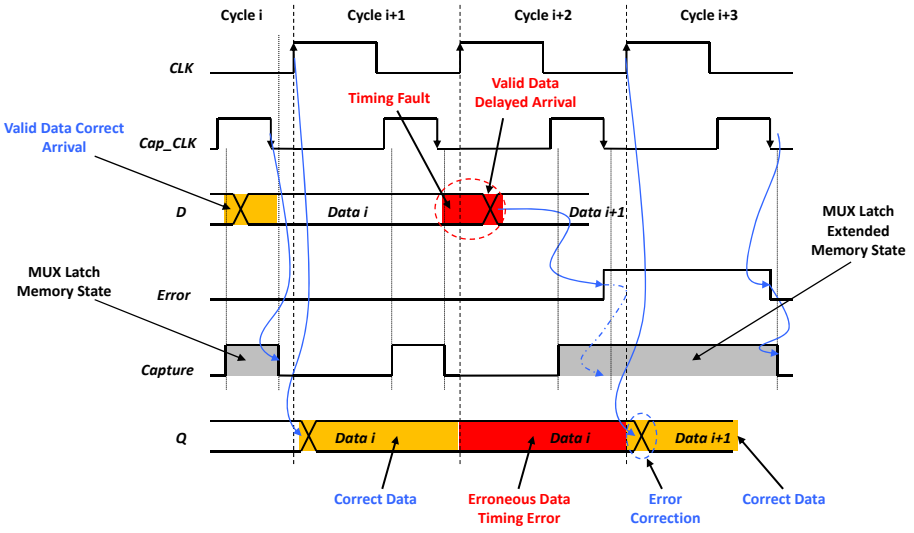
The Time Dilation Operation (II)



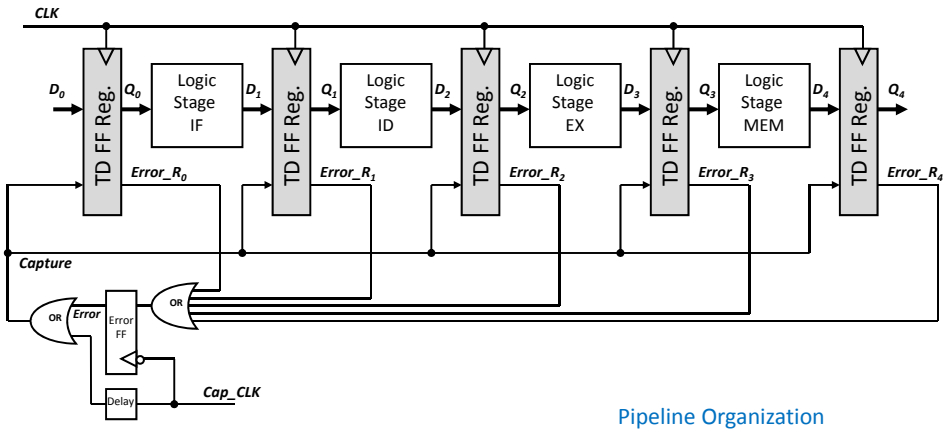
Erroneous Case

- No error detection latency!
- One clock cycle cost for error correction!

Timing Diagrams

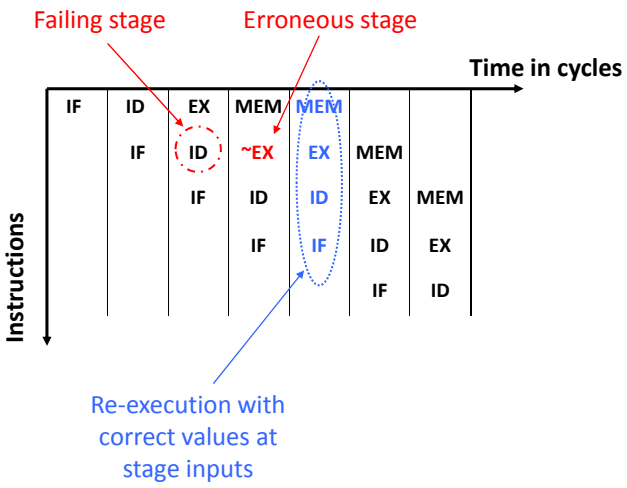


The Time Dilation Architecture



Pipeline Organization

Pipeline Recovery



References

- "*Making Typical Silicon Matter with Razor*", T. Austin, D. Blaauw, T. Mudge and K. Flautner, *IEEE Computers*, vol. 37, no. 3, pp. 57-65, 2004.
- "*Robust System Design with Built-In Soft-Error Resilience*", S. Mitra, N. Seifert, M. Zhang, Q. Shi and K-S. Kim, *IEEE Computers*, vol. 38, no. 2, pp. 43-52, 2005.
- "*Built-In Soft Error Resilience for Robust System Design*," S. Mitra et al, International Conference on IC Design and Technology, pp. 263-268, 2007.
- "*GRAAL: A New Fault Tolerant Design Paradigm for Mitigating the Flaws of Deep Nanometric Technologies*," M. Nicolaidis, International Test Conference, p. 4.3, 2007.
- "*Testing and Reliable Design of CMOS Circuits*", N. Jha and S. Kundu, *Kluwer Academic Publishers*, 1990.