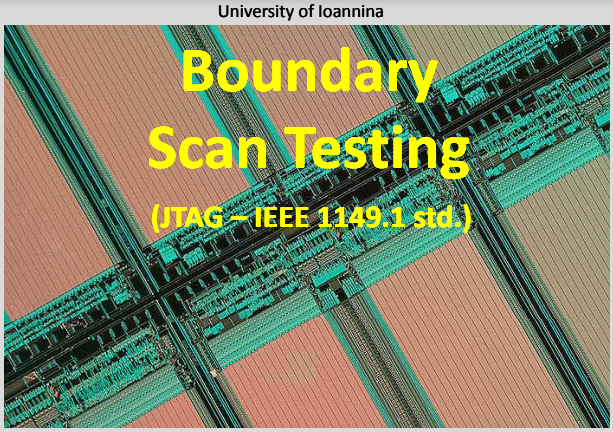
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

University of Ioannina



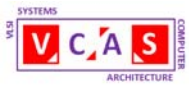
Boundary Scan Testing

(JTAG – IEEE 1149.1 std.)

Dept. of Computer Science and Engineering

Y. Tsiatouhas

CMOS Integrated Circuit Design Techniques

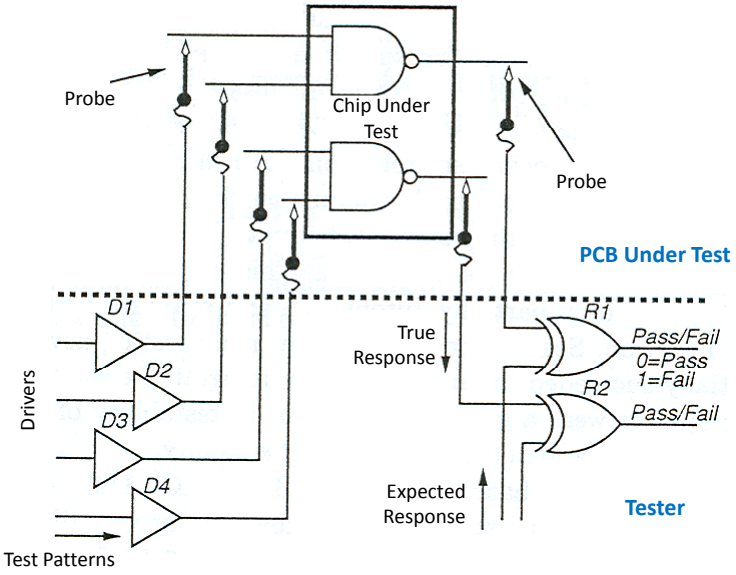


VLSI Systems
and Computer Architecture Lab

Overview

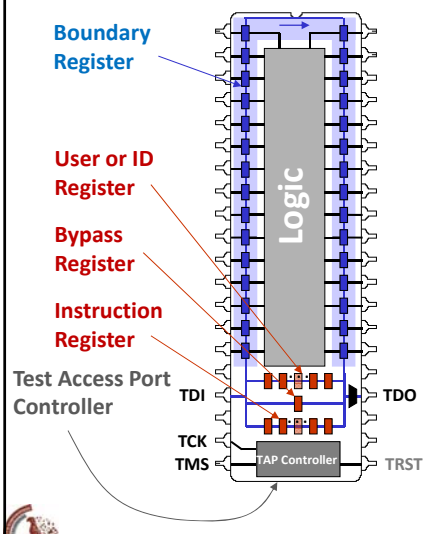
1. *Basic JTAG architecture*
2. *The Test Access Port (TAP)*
3. *JTAG registers*
4. *State diagram – Operating modes*
5. *Instruction set*
6. *External and internal testing operations*

Typical PCB Testing



Basic JTAG Architecture (I)

(IEEE 1149.1 std)

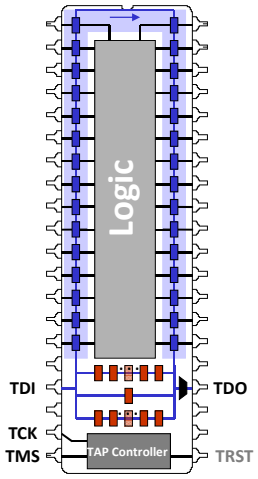


The JTAG 1149.1 Boundary Scan std. supports PCB testing procedures according to a commonly acceptable (standard) test mechanism.

It consists of:

- A *Test Access Port - TAP* with 4 or 5 pins.
- A set of registers (an *instruction register* (*IR*), a *bypass register* (*BR*) and *data registers* (*DR*).
- A *TAP Controller* which is a finite state machine (FSM) with 16 states.

Basic JTAG Architecture (II)

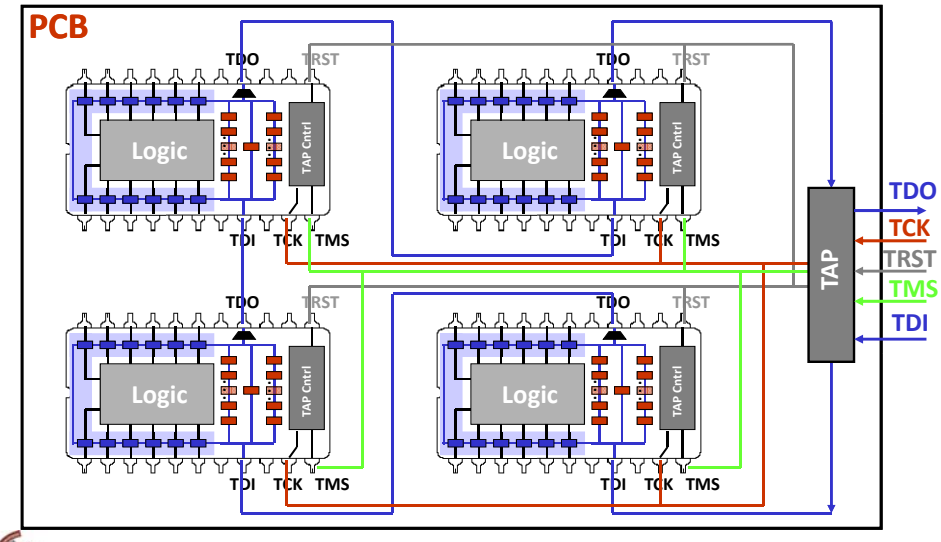


In the normal mode of operation the JTAG circuitry is transparent to the chip under test and the PCB system where this chip is embedded.

Two test modes of operation exist:

- Internal Testing where the internal logic of the chip is tested.
- External Testing where the interconnections among the chips are tested.

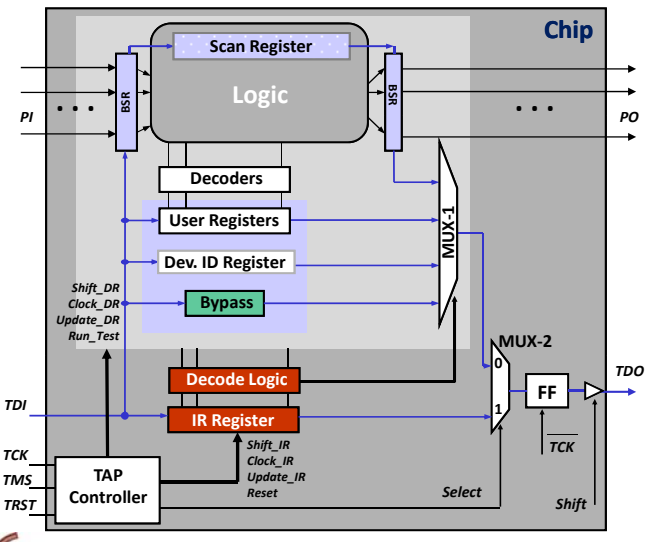
Test Access Port – TAP (I)



Test Access Port – TAP (II)

- TCK (Test Clock): This is the test clock signal, which synchronizes the test procedure independently of the system clock. Under the control of this signal test data are shifted between the TAP registers.
- TDI (Test Data Input): Serial test data input. New data are scanned-in at each positive edge of the TCK clock signal. When not in use must remain at logic High.
- TDO (Test Data Output): Serial test data output. Data are scanned-out at the negative edge of the TCK clock signal.
- TMS (Test Mode Select): The sequence of values at this input is translated by the TAP Controller and is used to control the test procedure. When not in use must remain at logic High.
- TRST (Test Reset): This is an optional signal, which is used for the asynchronous initialization of the test logic independently of the clock signal TCK.

Registers



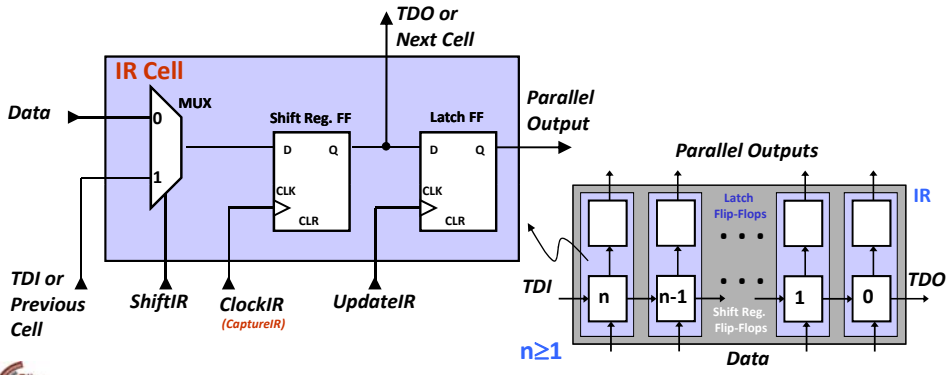
The JTAG protocol provides the ability to support a large number of user defined registers. However, the presence of three registers is mandatory :

- Bypass Register (BR) (*Καταχωρητής Παράκαμψης*)
- Instruction Register (IR) (*Καταχωρητής Εντολών*)
- Boundary Scan Register (BSR) (*Καταχωρητής Περιφερειακής Σάρωσης*)

Instruction Register – IR

(Καταχωρητής Εντολών)

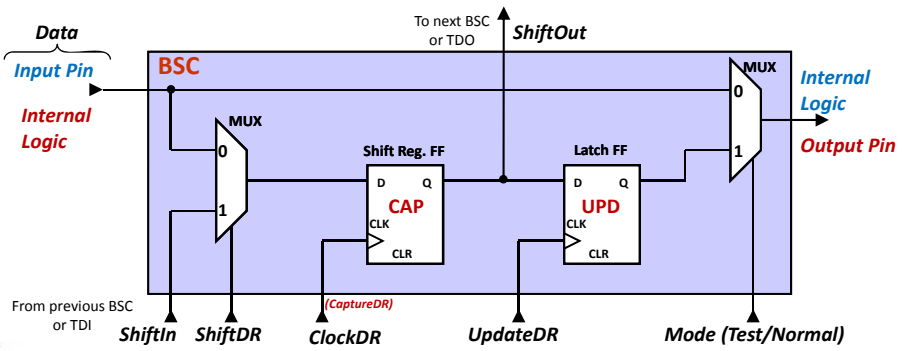
- The *Instruction Register – IR* (*Καταχωρητής Εντολών*) is a serial / parallel input and output register. Each stage of the register consists of a pair of a flip-flop and a latch. The flip-flop feeds the corresponding latch. The latch holds the current instruction when the IR is updated with new data (instructions). The size of the register is at least two bits.



Boundary Scan Register – BSR

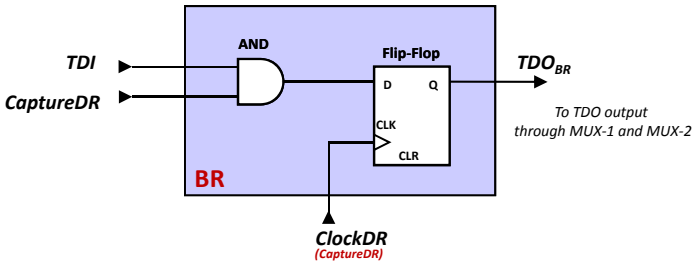
(Καταχωρητής Περιφερειακής Σάρωσης)

- The *Boundary Scan Register – BSR* (*Καταχωρητής Περιφερειακής Σάρωσης*) is placed at the chip periphery, in-between the input/output pads and the internal logic. It consists of the *Boundary Scan Cells – BSC* (*Κύτταρα Περιφερειακής Σάρωσης*) and supports both the testing of the internal logic of the chip as well as the interconnects of the chip with other chips.



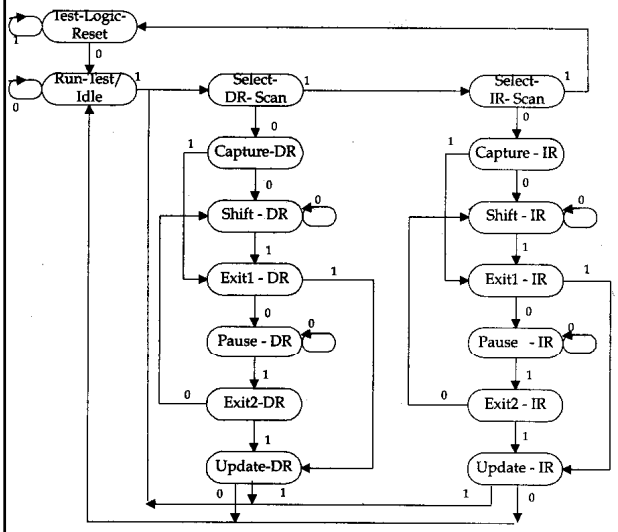
Bypass Register – BR

- The *Bypass Register – BR* (*Καταχωρητής Παράκαμψης*) is an one bit register consisting of a single Flip-Flop*. It permits the signal at the TDI input to bypass the BSR register and directly feed the TDO output.



** In practice the BR is implemented as a single boundary scan cell !*

TAP Controller State Diagram



The TAP controller is a Finite State Machine (FSM) with 16 states. The state transition takes place at the positive edge of the TCK clock signal.

At the state diagram beside, the arrows between the states are marked with 0 or 1, which correspond to the logic level that the TMS signal must have before the positive edge of the clock signal TCK in order to activate the corresponding state transition.

Modes of Operation

Two basic modes of operation exist for the JTAG 1149.1 std. and each mode supports specific instructions:

- *Non-Invasive Mode* (*Απρόσκοπτος Τρόπος*): The TAP controller and the pertinent port operate asynchronously and independently with respect to the system under test. In this mode, the TAP port can be exploited without disturbing the operation of the system.
- Pin Permission Mode (*Τρόπος Επίτρεψης Ακροδέκτη*): In this mode, the internal logic of the circuit under test is disconnected from the input/output pins. Consequently, only testing operations can be performed.

Instruction Set – I

(Non-Invasive)

- ***BYPASS***: This instruction places the 1-bit bypass register between the TDI and TDO pins. The BYPASS instruction is mandatory for the protocol. The all ones state in the instruction register must correspond to this instruction.
- ***IDCODE***: This instruction places a 32-bit register between the TDI and TDO pins. The register is loaded in parallel by the hardware with the code ID of the chip.
- ***USERCODE***: Once again, this instruction places the previous 32-bit register between the TDI and TDO pins. This time the register is not loaded with the code ID of the chip but with a user defined code. This instruction is related to programmable devices (like FPGAs).

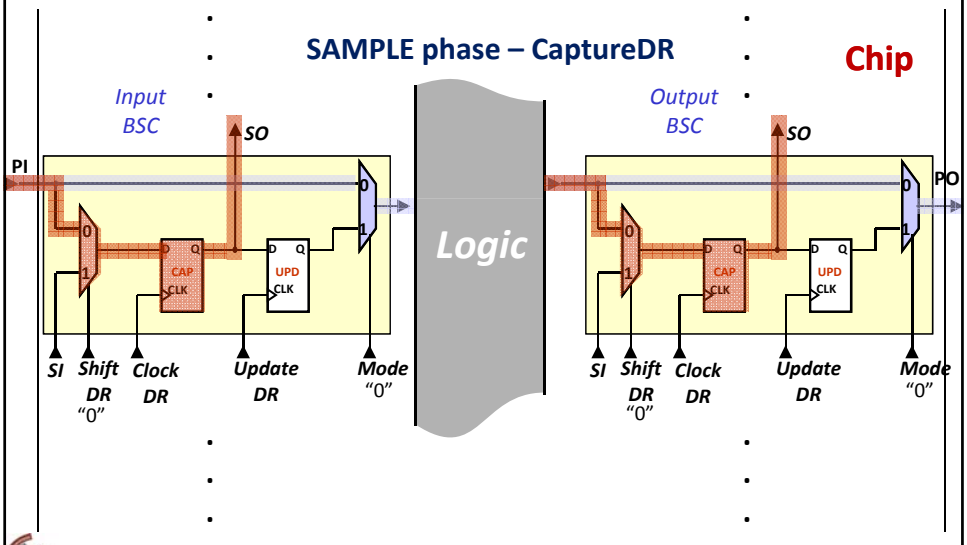
Instruction Set – II

(Non-Invasive)

- ***SAMPLE/PRELOAD instruction***: This instruction places the boundary scan register (BSR) between the TDI and TDO pins. This instruction is mandatory for the protocol. The Sample/Preload instruction does not disturb the normal mode of operation since the *Mode* signal of the second multiplexer in the boundary scan cells is at logic "0" (normal mode). The instruction activates two operations:
  - The SAMPLE operation is accomplished at the CAPTURE-DR state of the TAP controller where the CAP Flip-Flops capture the data at their inputs. Thus, the BSR register holds a snapshot of the activity at the chip's I/Os. Then, the sampled data can be scanned-out for observation.
  - The PRELOAD operation is accomplished during the scan-out activity, where in parallel new data are scanned-in. Thus, the data at the ShiftIn (SI) inputs are captured by the CAP Flip-Flops and subsequently feed the UPD Flip-Flops when the TAP controller is at the UPDATE-DR state.

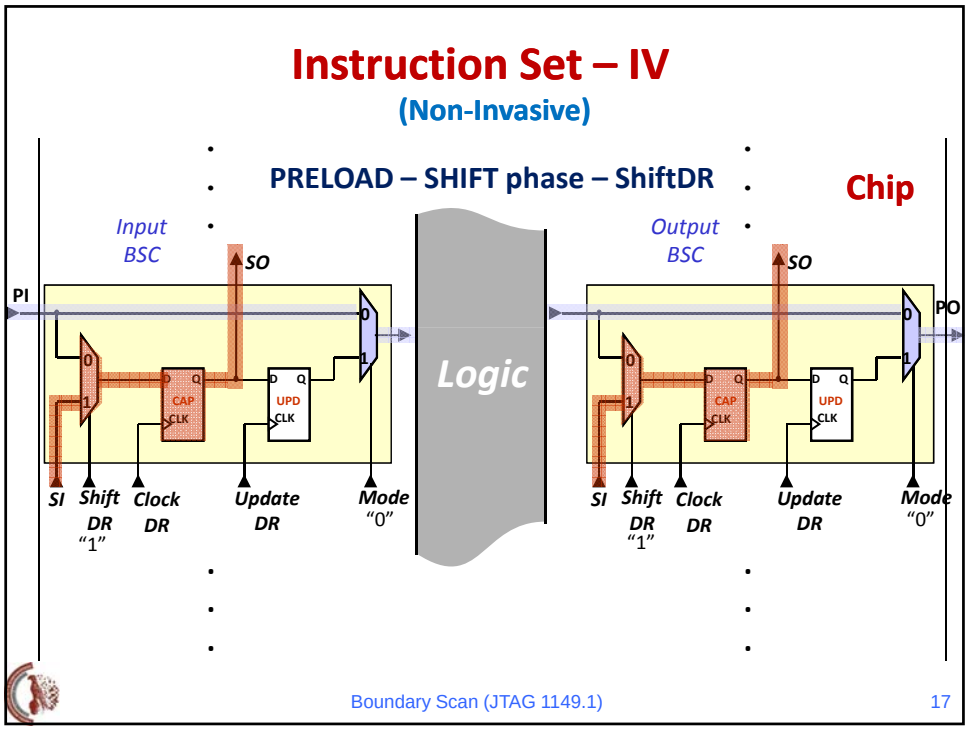
Instruction Set – III

(Non-Invasive)



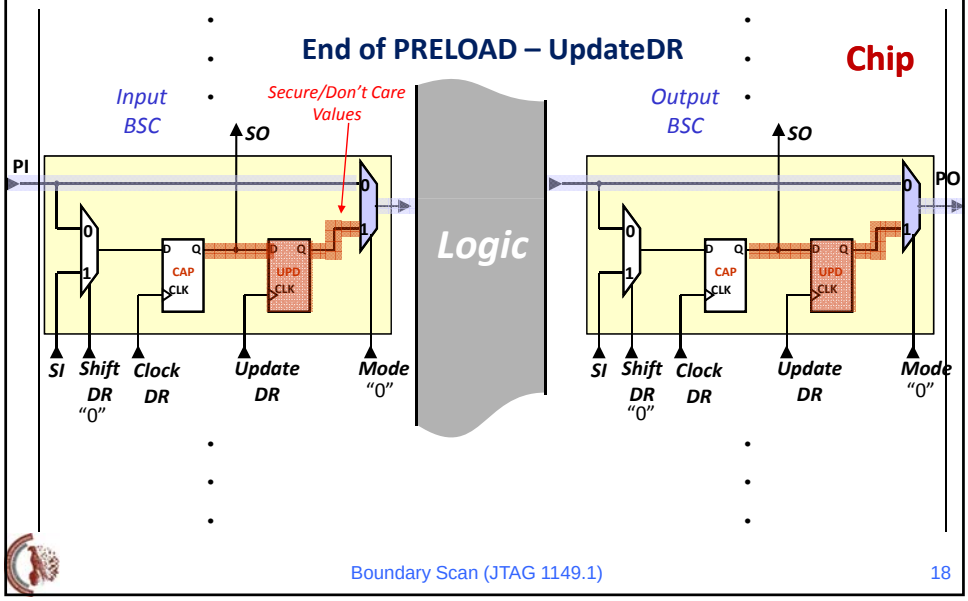
Instruction Set – IV

(Non-Invasive)



Instruction Set – V

(Non-Invasive)



Instruction Set – VI

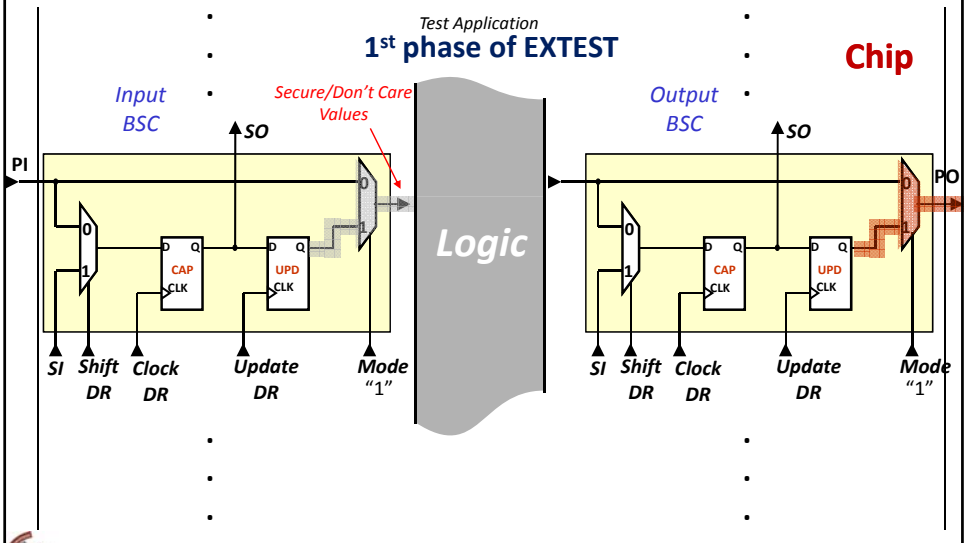
(Pin-Permission)

- ***The EXTEST instruction***: This instruction places the boundary scan register between the TDI and TDO pins. The instruction is *mandatory* and the all zero state at the instruction register must correspond to it.

  At the CAPTURE-DR state, the logic values at the input pads of the chip are captured in the CAP Flip-Flops of the BSC cells. In addition, the output pads are driven by the UPD Flip-Flops since the *Mode* signal is "1". With this instruction the input pads are sampled and the output pads are driven. Consequently, at the shift operations on the BSR register, the state of the input pads is read while new values are set at the output pads of the chip.

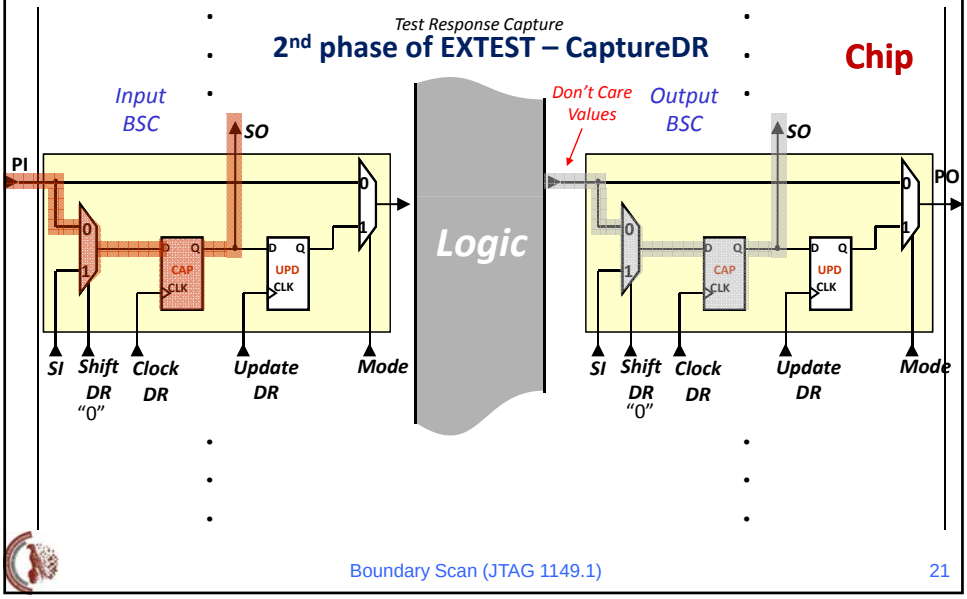
Instruction Set – VII

(Pin-Permission)



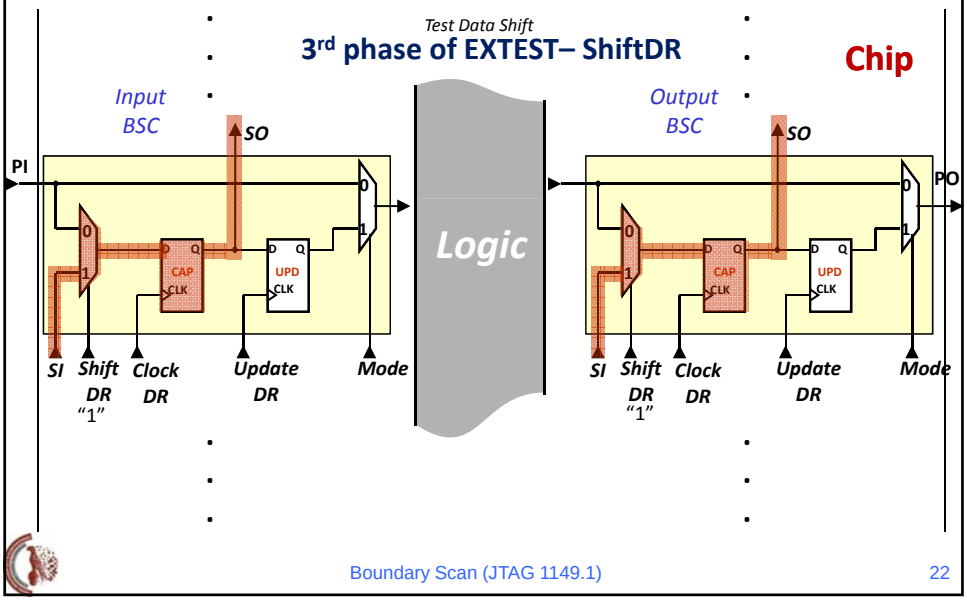
Instruction Set – VIII

(Pin-Permission)



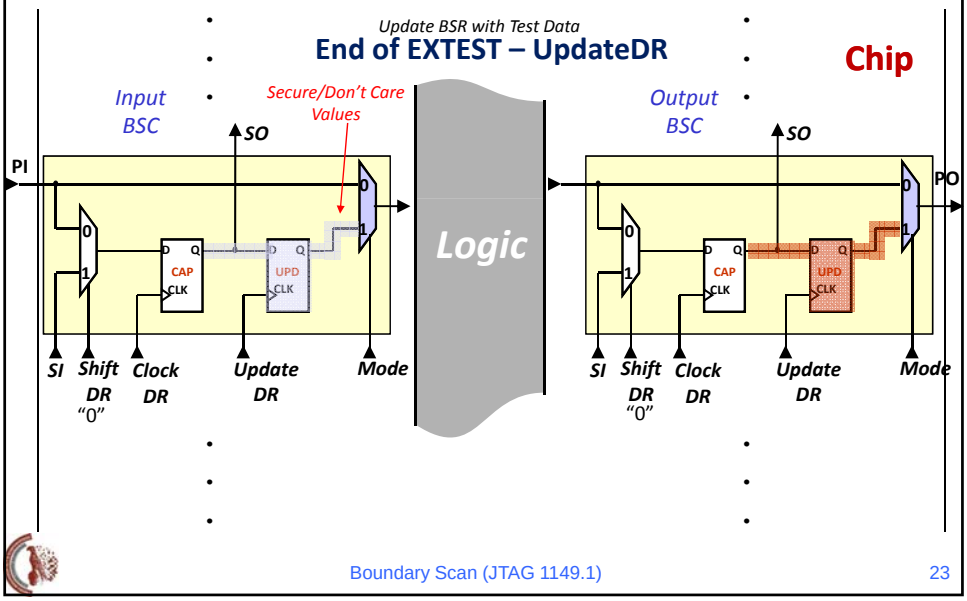
Instruction Set – IX

(Pin-Permission)



Instruction Set – X

(Non-Invasive)



Instruction Set – XI

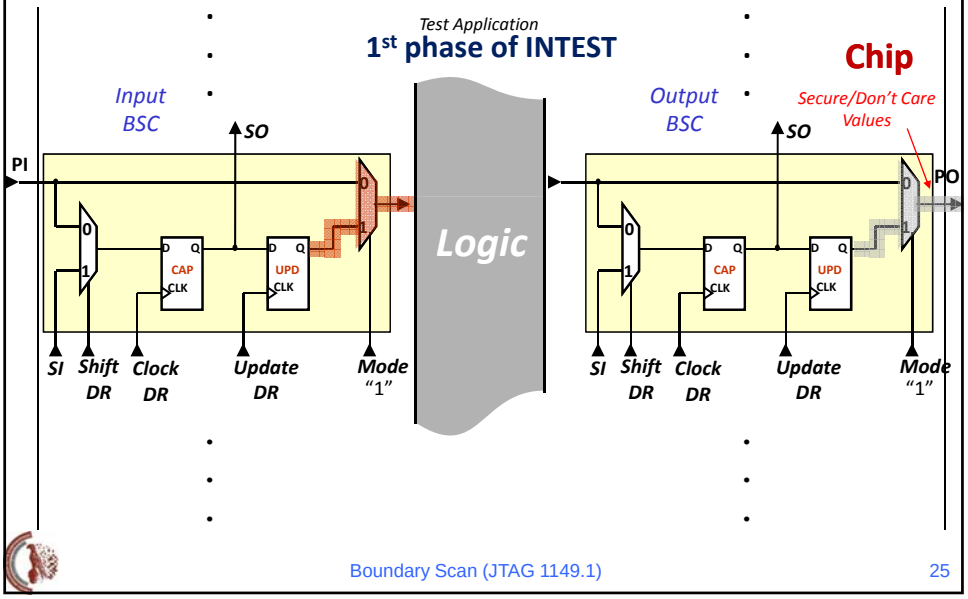
(Pin-Permission)

- ***The RUNBIST instruction***: This instruction activates a user defined register which may be one of the existing registers in the protocol. The target is to permit the use of embedded BIST techniques. The BIST procedures start when the TAP controller is at the RUN-TEST-IDLE state.

- ***The INTEST instruction***: This instruction places the boundary scan register between the TDI and TDO pins. It sets the inputs of the internal logic under the control of the corresponding UPD Flip-Flops of the BSR. In addition, the BSR cells at the outputs of the internal logic sample the corresponding responses at the CAPTURE-DR state. Consequently, at the UPDATE-DR state a test pattern is applied while at the CAPTURE-DR state the response of the logic to this pattern is sampled. Next, the response is scanned-out and concurrently a new test pattern is scanned-in.

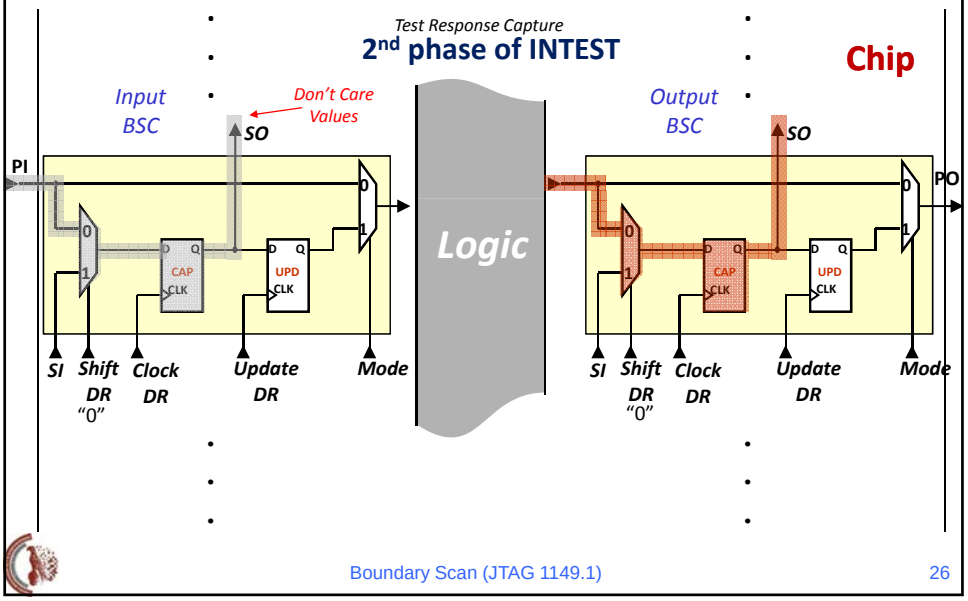
Instruction Set – XII

(Pin-Permission)



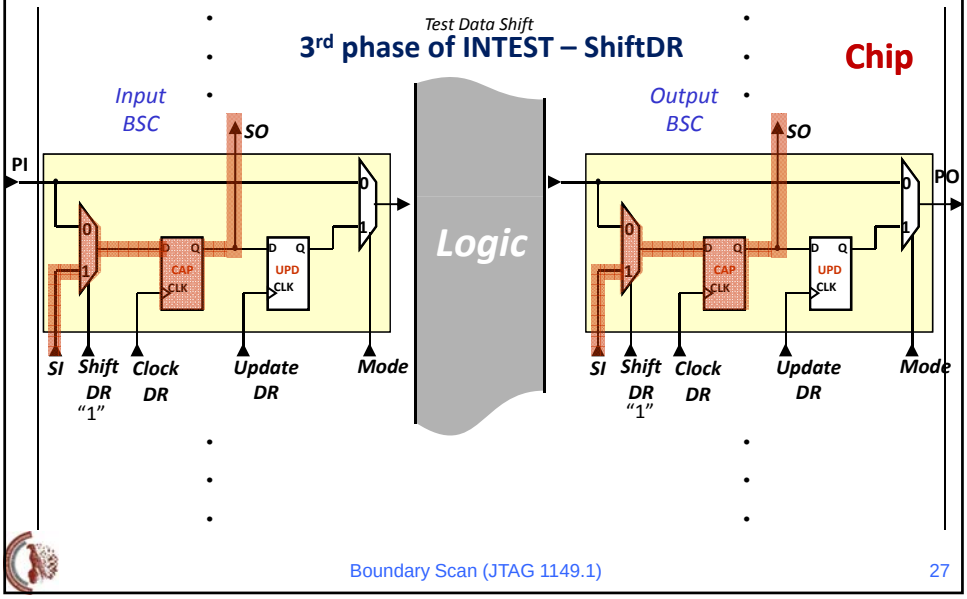
Instruction Set – XIII

(Pin-Permission)



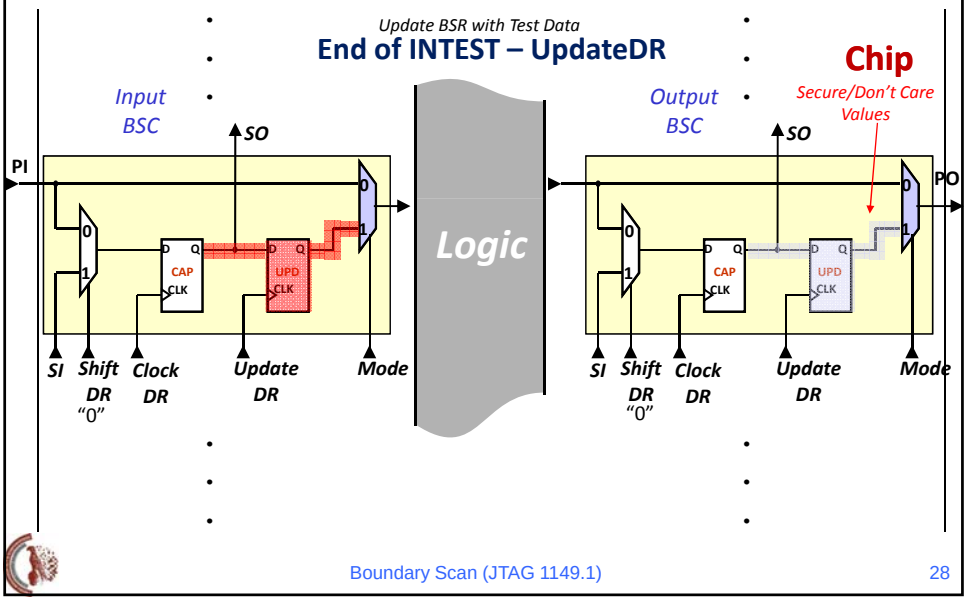
Instruction Set – XIV

(Pin-Permission)



Instruction Set – XV

(Non-Invasive)



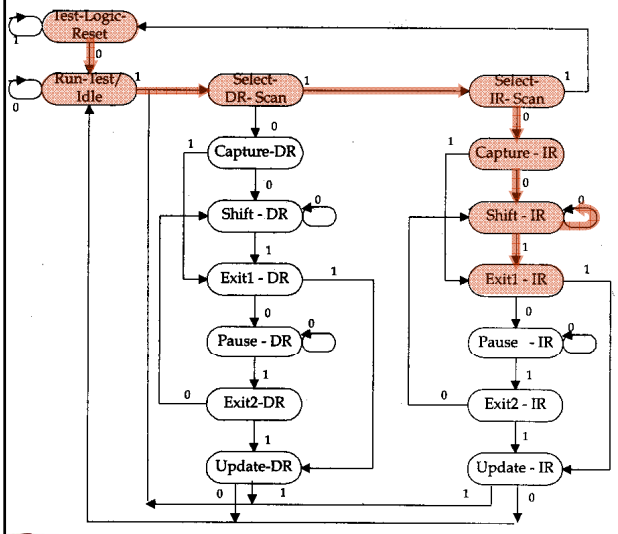
Instruction Set – XVI

(Pin-Permission)

- ***The HIGHZ instruction***: This instruction places the bypass register between the TDI and TDO pins. In addition, sets the output pads in the "high Z" condition at the UPDATE-IR state. It is exploited for the testing of chips that are not compliant with the JTAG protocol.

- ***The CLAMP instruction***: This instruction places the bypass register between the TDI and TDO pins. In addition, sets the output pads under the control of the BSR register, which has been earlier fed with proper values by exploiting a sequence of SAMPLE/PRELOAD instructions. Consequently, the output pads of the chip retain specific values during the testing procedures that are applied to other chips where these outputs do not participate.

Instruction Register Update – I



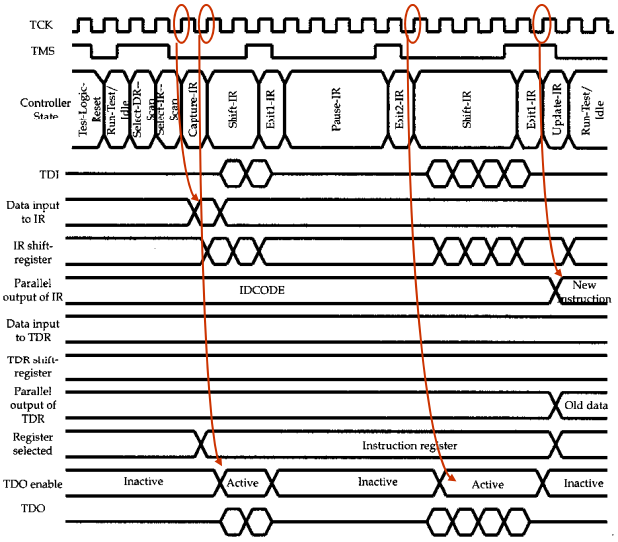
Initialization at the TEST-LOGIC-RESET state by exploiting the TRST signal.

Proper use of the TMS and TCK signals in order to activate the CAPTURE-IR state and subsequently the SHIFT-IR state.

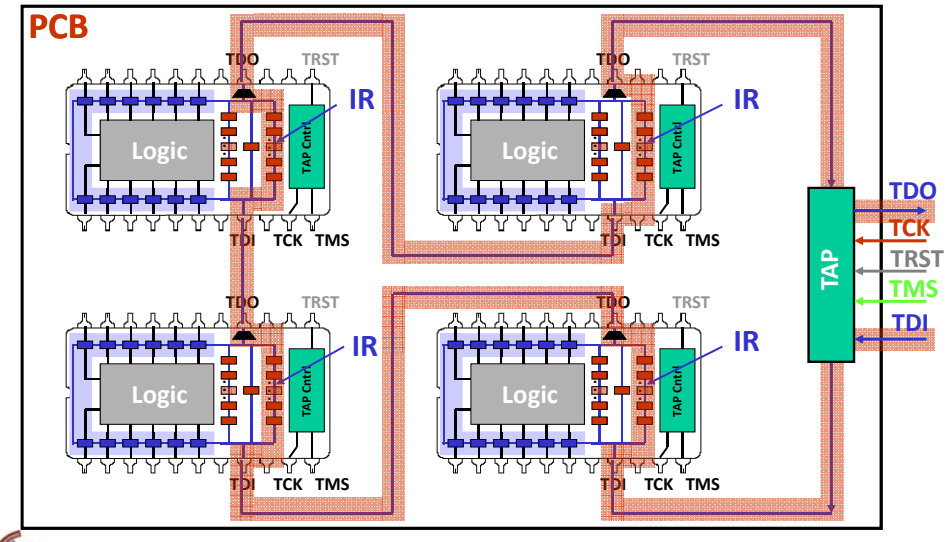
At the CAPTURE-IR state the IR register is placed between the TDI and TDO pins.

At the SHIFT-IR state the TDO pin is activated.

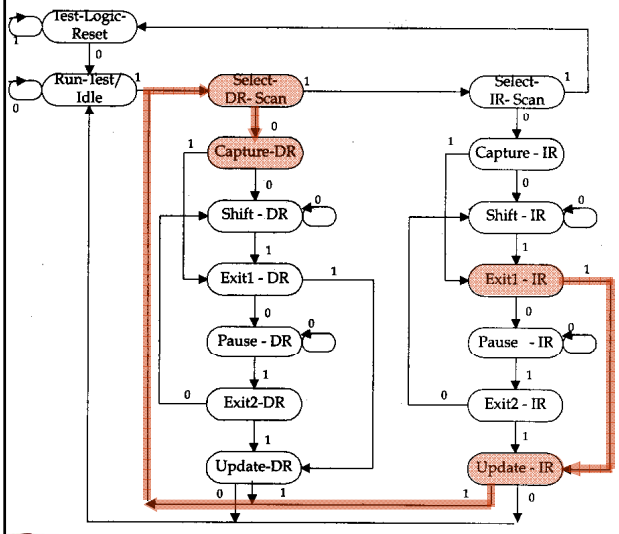
Instruction Register Update – II



Instruction Register Update – III

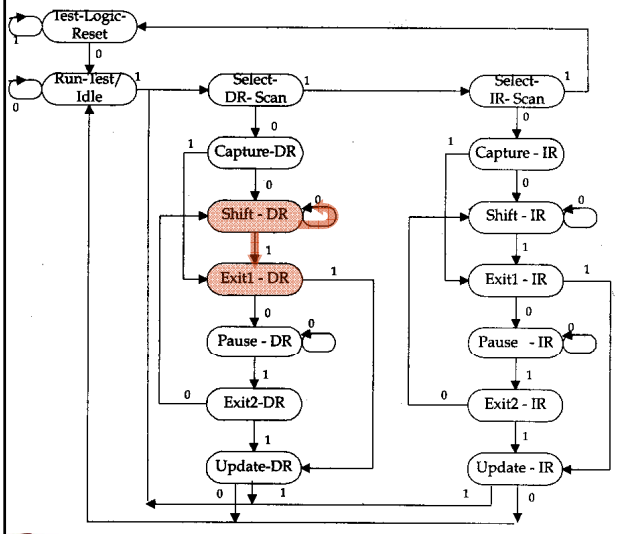


Data Register Activation



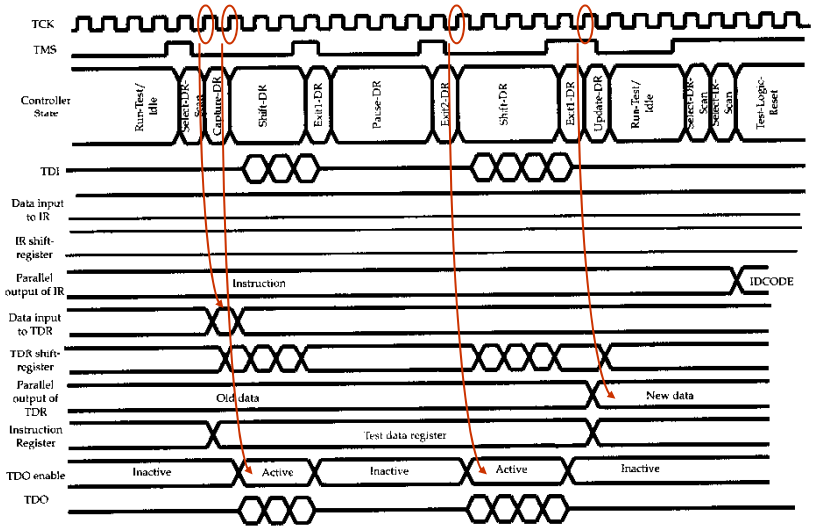
The update of the IR register, at the UPDATE-IR state, will result to the connection of the proper data register between the TDI and TDO pins when the TAP controller will be at the CAPTURE-DR state.

Data Register Update – I



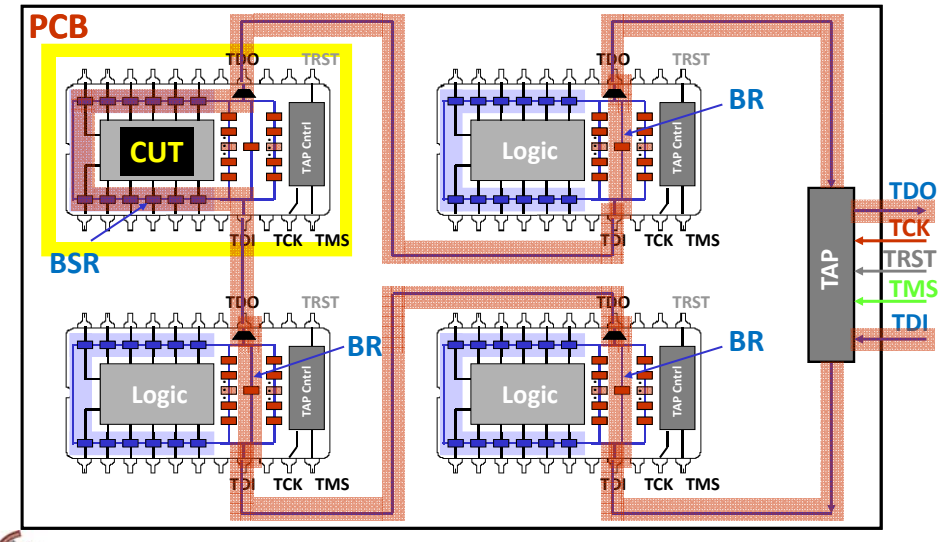
At SHIFT-DR state the TDO is activated and new test data are scanned-in/out to the selected register.

Data Register Update – II

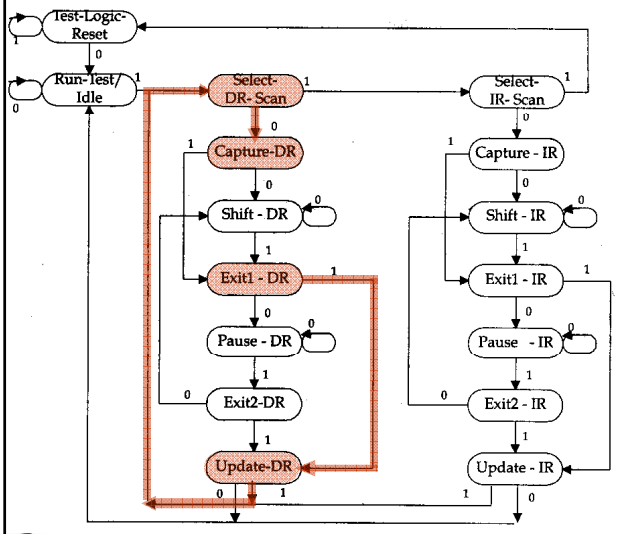


Data Register Update – III

(& Bypass Operation)



Data Register Activation



At the UPDATE-DR state the data register is updated.

Possibly another data shift phase will be initiated next.

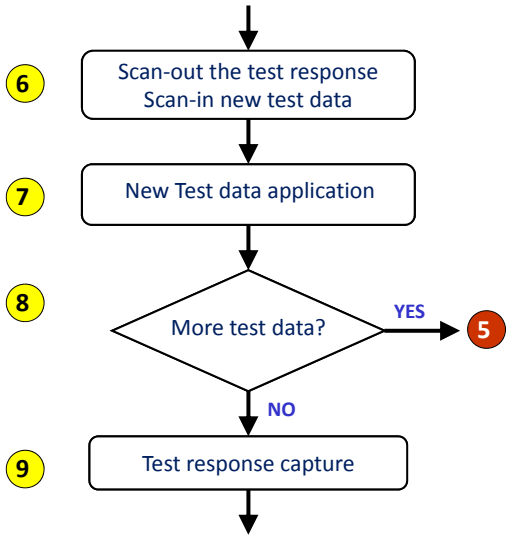
Basic Testing Procedure – I

(External or Internal Testing)

1. TEST-LOGIG-RESET
2. Load IR with the instruction SAMPLE/PRELOAD
   - Invasive Mode - The selected DR is placed between TDI-TDO
3. Shift data to the selected DR (e.g. BSR)
   PRELOAD phase
4. Load IR with the instruction EXTEST ή INTEST
   - Pin-Permission Mode - The selected DR is placed between TDI-TDO. Test data application.
5. Test response Capture

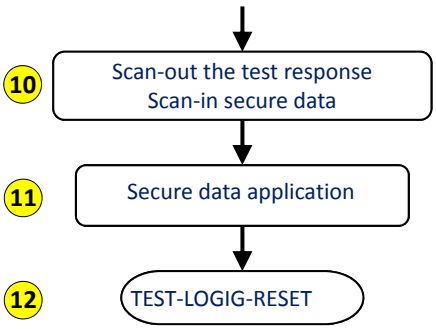
Basic Testing Procedure – II

(External or Internal Testing)



Basic Testing Procedure – III

(External or Internal Testing)



IEEE P1687 – Internal JTAG (IJTAG)

IEEE P1687 std.

Also referred to as IJTAG (Internal JTAG), the IEEE P1687 working group intends to develop a methodology for access to embedded test and debug features (but not the features themselves) via the IEEE 1149.1 Test Access Port (TAP) and additional signals that may be required. The IEEE 1149.1 standard specifies circuits to be embedded within a Integrated Circuit to support board test, namely the Test Access Port (TAP), TAP Controller, and a number of internal registers. In practice, the TAP and TAP controller are being used for other functions well beyond boundary scan in an ad-hoc manner across the industry to access a wide variety of internal chip test and debug features. The purpose of the IJTAG initiative is to provide an extension to the IEEE 1149.1 standard specifically aimed at using the TAP to manage the configuration, operation and collection of data from embedded test and debug circuitry. There exists the widespread use of embedded instrumentation (such as BIST Engines, Complex I/O Characterization and Calibration, Embedded Timing Instrumentation, etc.) each of which is accessed and managed by a variety of external instrumentation using a variety of mechanisms and protocols. Therefore, there exists a need for a standardization of these protocols in order to ensure an efficient and orderly methodology for the preparation of tests and the access and control of these embedded instruments. The elements of the methodology include a description language for the characteristics of the features and for communication with the features, and requirements for interfacing to the features.

Source: IEEE

References

- "*The Boundary-Scan Handbook*," K. Parker, Kluwer Academic Publishers, 1992.
- "*Principles of Testing Electronics Systems*", S. Mourad and Y. Zorian, *John Wiley & Sons*, 2000.
- "*Essentials of Electronic Testing: for Digital, Memory and Mixed-Signal VLSI Circuits*", M. Bushnell and V. Agrawal, Kluwer Academic Publishers, 2000.
- "*System-on-Chip Test Architectures*", L-T Wang, C. Stroud and N. Touba, Morgan-Kaufmann, 2008.