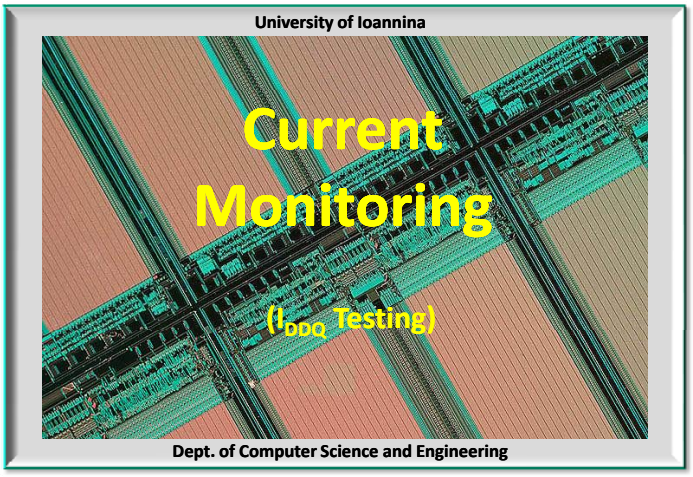
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES



Y. Tsiatouhas

CMOS Integrated Circuit Design Techniques

VLSI Systems
and Computer Architecture Lab

Overview

1. *The I_{DDQ} testing technique*
2. *Influence of defects in CMOS circuits*
3. *A typical I_{DDQ} testing scheme*
4. *I_{DDQ} testing and technology evolution*
5. *I_{DDQ} testing improvements*

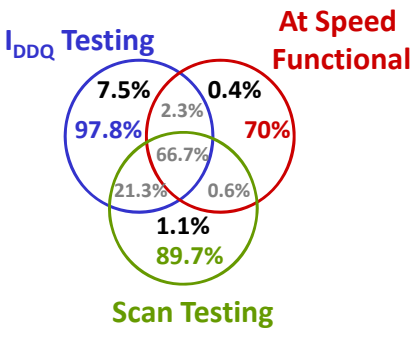
The I_{DDQ} Testing Technique

Theoretically, the current monitoring (I_{DDQ} testing) technique is one of the most effective techniques for the discrimination of defect free from defective circuits.

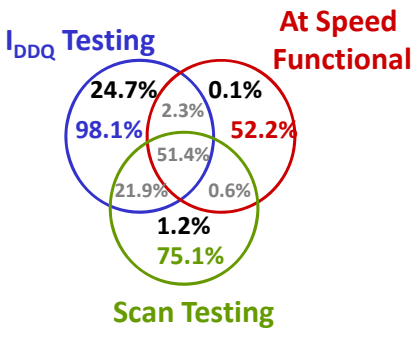
It is based on the observation that a defect free CMOS integrated circuit has a quite small quiescent current (I_{DDQ} current) in the steady state (due to transistor current leakages), with respect to a defective one.

In case that the measured quiescent current is much higher than the expected level (taking into account possible variations), then the circuit is considered as defective. The additional current is due to possible short circuits.

I_{DDQ} Testing Advantages



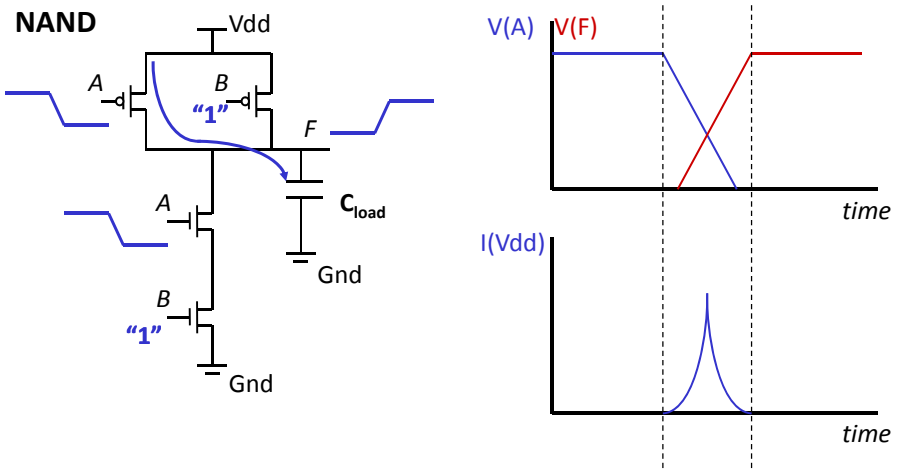
HP Data



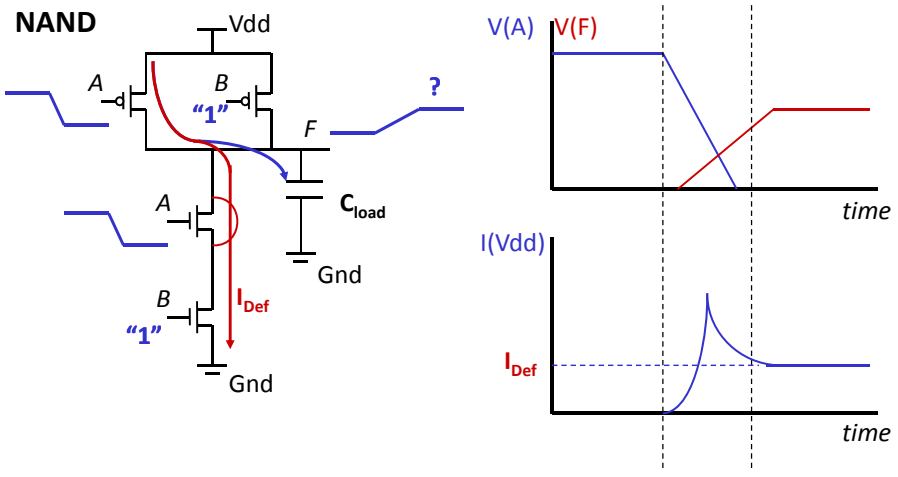
IBM Data

Defect Detection by using ~100 vectors

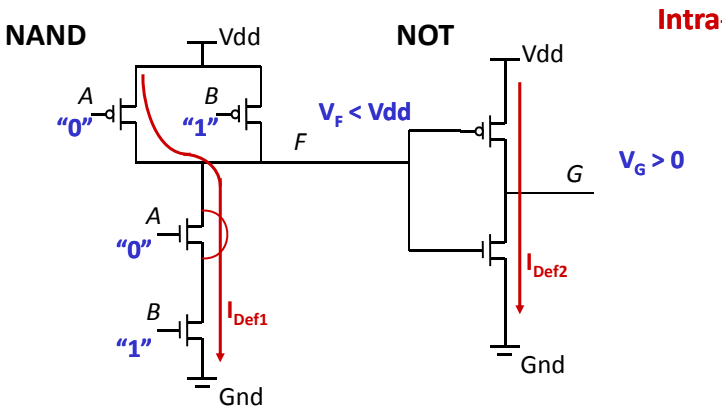
CMOS Logic Circuit Operation



CMOS Circuit Defects

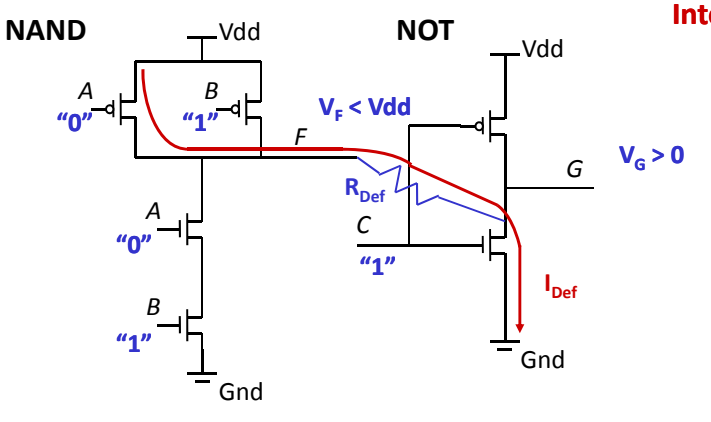


Side Effects



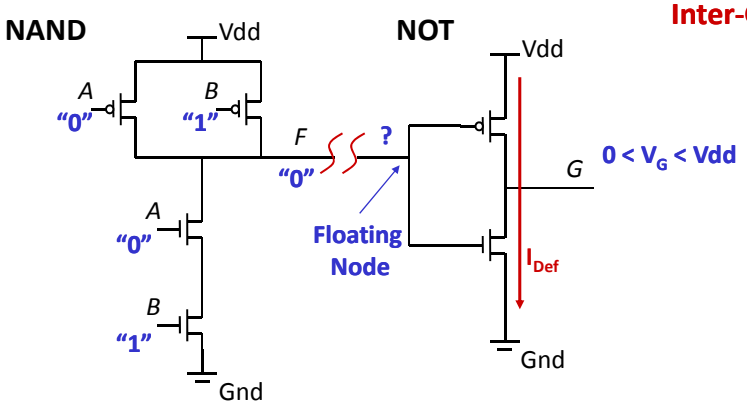
$I_{Def} = I_{Def1} + I_{Def2}$

Other Defect Cases (I)

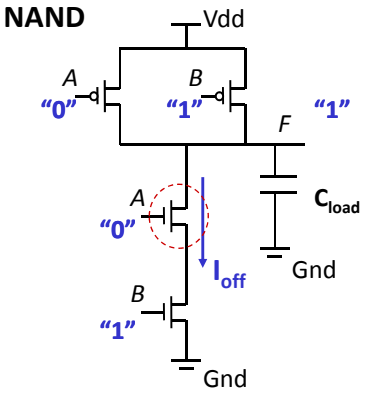


Other Defect Cases (II)

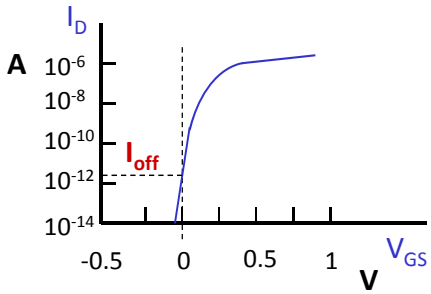
Inter-Gate Open



Quiescent Current – I_{DDQ}

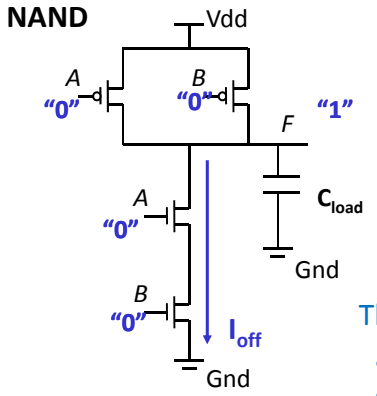


$$I_{off} = \mu C_{ox} \frac{W}{L} V_T^2 e^{\frac{V_{GS}-V_{th}}{\eta V_T}}$$



The I_{DDQ} current is the sum of all I_{off} & I_{Def} currents in the quiescent state of a circuit

I_{DDQ} Current Dependencies

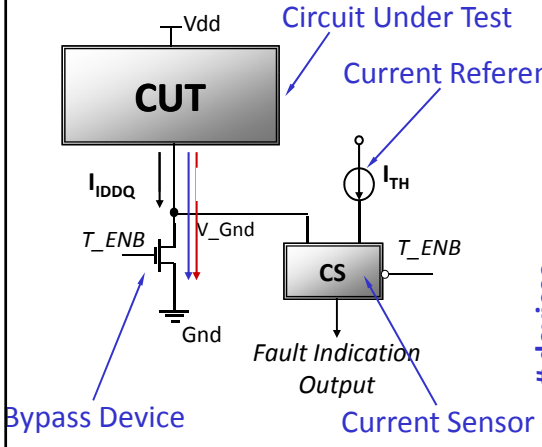


$$I_{off} = \mu C_{ox} \frac{W}{L} V_T^2 e^{\frac{V_{GS}-V_{th}}{\eta V_T}}$$

The I_{DDQ} current strongly depends on:

- Process variations
- Temperature variations
- The applied input vector

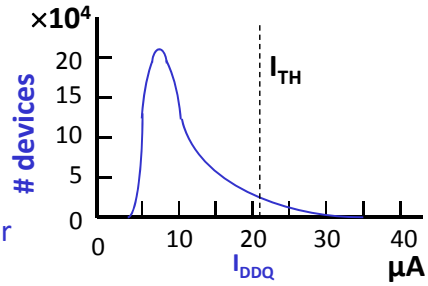
A Typical I_{DDQ} Testing Scheme



$I_{IDDQ} = I_B + I_{Def}$

$I_B = \Sigma I_{off}$

$I_{B\text{-}max} << I_{TH} < I_{Def\text{-}min}$



I_{DDQ} Testing Challenges (I)

Year
Technology node
Physical gate length (high perform.)
EOT: Equiv. oxide thickness
Max. gate leakage current density
V_{DD}: power supply
V_{tsat}: Saturation threshold voltage
I_{off}: S/D subthreshold leakage current
I_{Dsat}: NMOS drive current
Mobility enhancement factor

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
L_g Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	12	11	11	10	9	8.5	8	8	
UTB FD (Å)				9	8	7	6	5	5
DG (Å)							6	5	5
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]									
Extended Planar Bulk (Å)	19.3	18.4	18.4	17.0	16.0	9.2	7.5	7.5	
UTB FD (Å)				11	10	11	10	9	9
DG (Å)							12	11	10
$J_{g\,max}$ Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm²)	1.88E+02	5.36E+02	8.00E+02	1.18E+03	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
UTB FD (A/cm²)				7.73E+02	9.50E+02	1.22E+03	1.38E+03	2.07E+03	2.23E+03
DG (A/cm²)							6.25E+02	7.86E+02	8.46E+02
V_{dd} Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
$V_{t,sat}$ Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	195	168	165	164	237	151	146	148	
UTB FD (mV)				148	148	167	170	166	167
DG (mV)							190	192	195
$I_{d,leak}$ Source-Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (pA/µm)	0.06	0.15	0.2	0.28	0.22	0.28	0.32	0.34	
UTB FD (pA/µm)				0.32	0.40	0.22	0.22	0.29	0.29
DG (pA/µm)							0.1	0.11	0.11
$I_{d,sat}$ effective NMOS Drive Current [9]									
Extended Planar Bulk (µA/µm)	1.02E+03	1.13E+03	1.26E+03	1.21E+03	1.18E+03	2.05E+03	2.49E+03	2.30E+03	
UTB FD (µA/µm)				1496	1640	1815	2015	2037	2198
DG (µA/µm)							1899	1932	2220
Mobility Enhancement Factor for $I_{d,sat}$ [10]									
Extended Planar Bulk	1.09	1.09	1.08	1.09	1.1	1.1	1.12	1.11	
UTB FD				1.08	1.08	1.08	1.06	1.05	1.05
DG							1.05	1.04	1.05

ITRS

International Technology Roadmap for Semiconductors

(*2006 Update*)

I_{DDQ} Testing Challenges (II)

Year
Technology node
Physical gate length (high perform.)
EOT: Equiv. oxide thickness
Max. gate leakage current density
V_{DD}: power supply
V_{tsat}: Saturation threshold voltage
I_{off}: S/D subthreshold leakage current
I_{Dsat}: NMOS drive current

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
L_g Physical L_{gate} for High Performance logic (nm) [1]	11	10	9	8	7	6	5
EOT: Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	5	5					
DG (Å)	6	6	5	5	5	5	5
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]							
Extended Planar Bulk (Å)							
UTB FD (Å)	9	9					
DG (Å)	10	10	9	9	9	9	9
$J_{g\,max}$ Maximum gate leakage current density [5]							
Extended Planar Bulk (A/cm²)							
FDSOI (A/cm²)	3.27E+03	3.70E+03					
DG (A/cm²)	1.00E+03	1.10E+03	1.22E+03	1.38E+03	1.57E+03	1.83E+03	2.20E+03
V_{dd} Power Supply Voltage (V) [6]	0.9	0.8	0.8	0.7	0.7	0.7	0.7
$V_{t,sat}$ Saturation Threshold Voltage [7]							
Extended Planar Bulk (mV)							
UTB FD (mV)	164	166					
DG (mV)	190	192	195	200	201	205	208
$I_{d,leak}$ Source-Drain Subthreshold Off-State Leakage Current [8]							
Extended Planar Bulk (pA/µm)							
UTB FD (pA/µm)	0.36	0.37					
DG (pA/µm)	0.11	0.11	0.11	0.11	0.11	0.11	0.11
$I_{d,sat}$ effective NMOS Drive Current [9]							
Extended Planar Bulk (pA/µm)							
UTB FD (pA/µm)	2290	2188					
DG (pA/µm)	2354	2275	2713	2533	2740	2744	2981

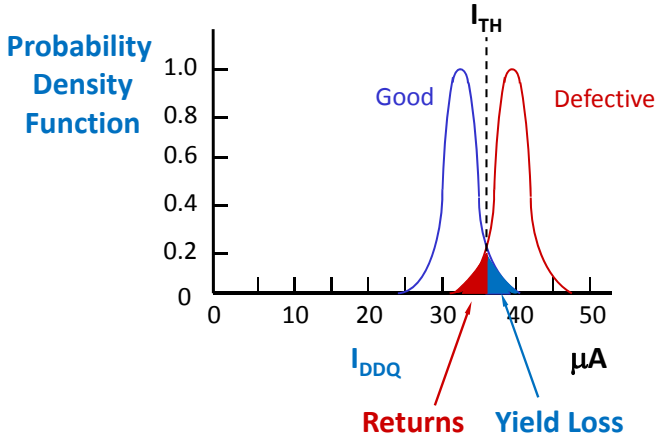
Technology Evolution and I_{DDQ} Testing

With technology evolution:

- the number of transistor/IC increases
- the intrinsic I_{DDQ} current increases
- the variations of I_{DDQ} current increases
- the level of the "defective" current that must be detectable decreases

The difficulty to discriminate the "defective" current from the intrinsic I_{DDQ} current in an IC is increased !

I_{DDQ} Testing Drawbacks



I_{DDQ} Testing Support (I)

Technology based techniques:

- Temperature lowering
- Separate power pins for sources, wells and substrate
- Reverse (back) bias techniques
- Multi-threshold transistors
- More independent power supply pins
- Circuit partition
- Built-in current sensors
- Silicon on Insulator (SOI) technology

Temperature Lowering

T (C)	St	Ioff (A)
-50	58.2	4.5E-13
0	72.6	2.9E-11
25	81.9	1.6E-10
75	96.6	2.5E-09

Intel

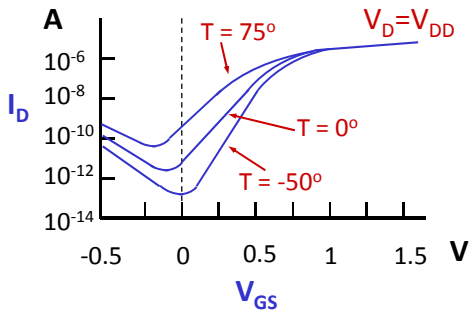
$$S_t = \ln 10 \left[\frac{KT}{q}\right] \cdot \left[1 + \frac{C_d}{C_{ox}}\right]$$

As temperature is lowered:

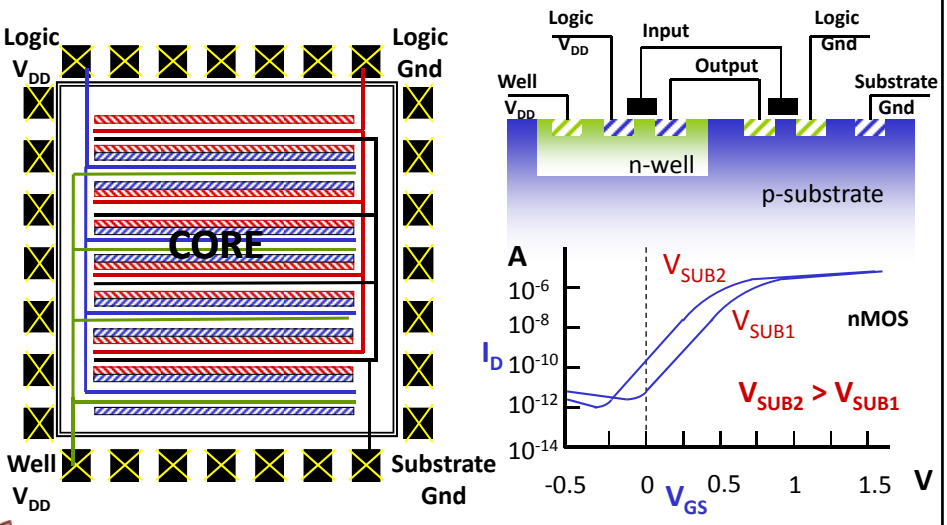
a) S_t linearly drops

b) V_{th} increases

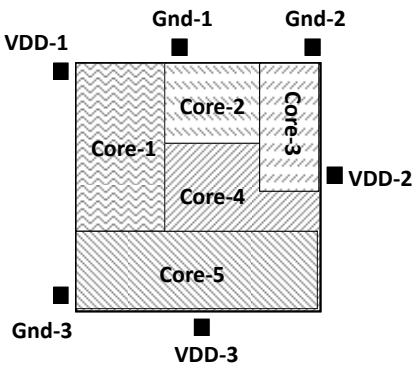
Since I_{Def} does not present an exponential decrease with the temperature I_{DDQ} testing can be performed at lower temperatures.



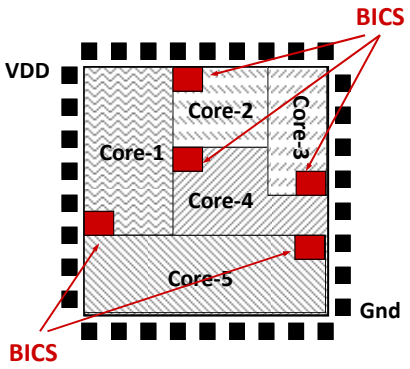
Separate Power Pins – Back Bias



Independent Power Pins – Partitioning



Core 1 - 2: VDD-1 & Gnd-1
Core 3 - 4: VDD-2 & Gnd-2
Core 5: VDD-3 & Gnd-3



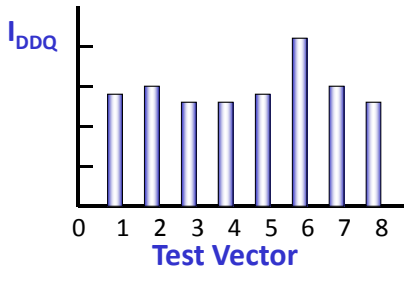
Use of Buit-In Current Sensors
BICS

I_{DDQ} Testing Support (II)

Test data analysis based techniques:

- ΔI_{DDQ} testing
- The current ratio technique
- Multi-parameter I_{DDQ} testing techniques
- Cluster analysis
- I_{DDQ} estimation based techniques
- Test vector selection

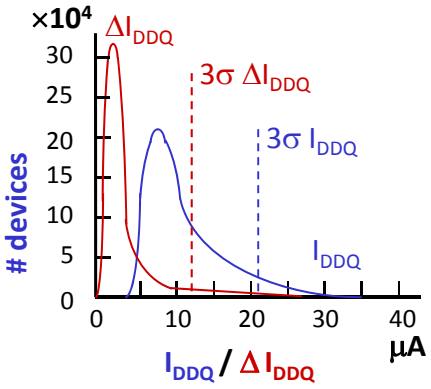
The ΔI_{DDQ} Testing Technique



$|I_{DDQ4} - I_{DDQ3}| \approx 0$

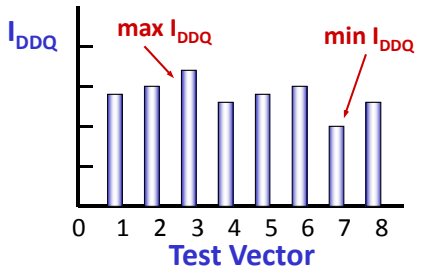
$|I_{DDQ5} - I_{DDQ4}| \approx 0$

$|I_{DDQ6} - I_{DDQ5}| \approx I_{Def}$



Current Ratios

Prototype Testing



$$\text{Current Ratio} = \alpha = \frac{\max I_{DDQ}}{\min I_{DDQ}}$$

Production Testing

a) For each die the I_{DDQ} current for the vector that provides the min I_{DDQ} is measured.

b) The measured min I_{DDQ} value is used to determine the max I_{DDQ} value exploiting the current ratio.

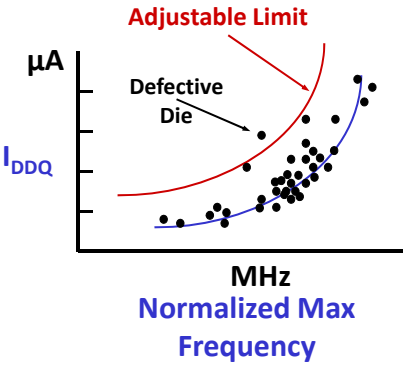
c) The calculated max I_{DDQ} value is used as the I_{TH} for the rest I_{DDQ} measurements.

Agilent

Multi-Parameter I_{DDQ} Testing Technique

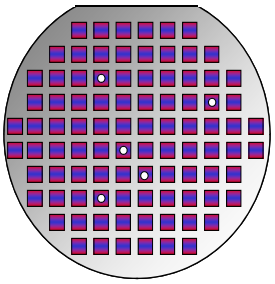
The maximum operating frequency F_{max} and the I_{DDQ} current can be used to discriminate fast (high frequency) dies and slow (low frequency) dies from defective dies.

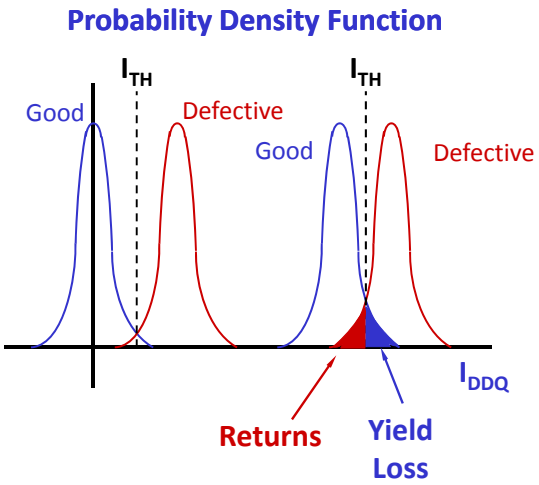
Decision Matrix		
IDDQ	**Fmax**	**Decision**
H	H	Good - Fast
H	L	Defective
L	H	Unlikely
L	L	Good - Slow



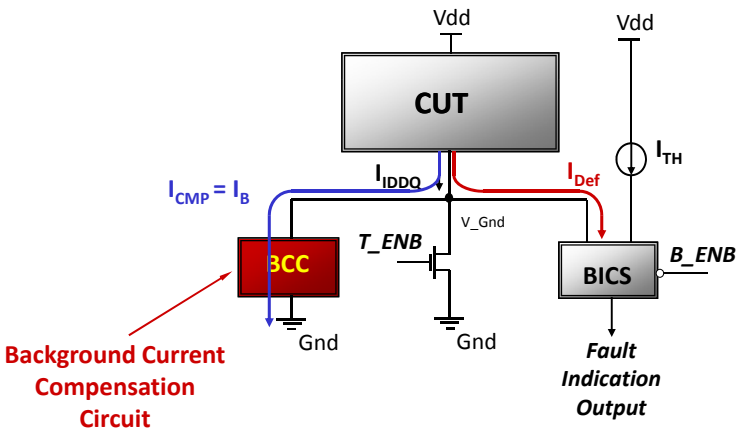
Intel

Cluster Analysis



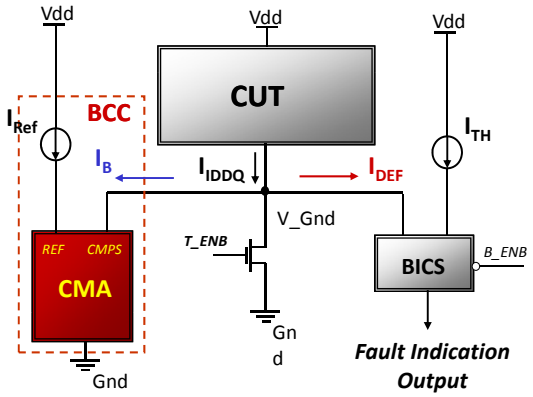


Background Current Compensation



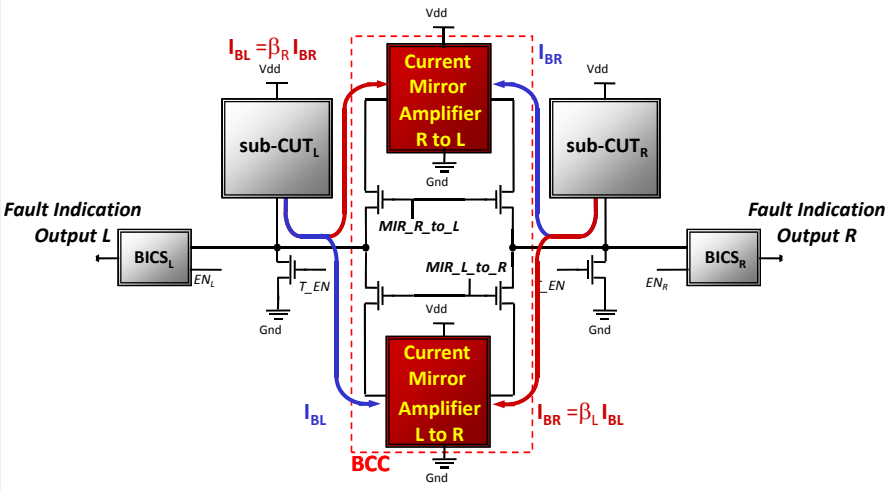
Higher Current Resolution
I_{TH} as low as BICS and/or BCC permit

Compensation Current Generation

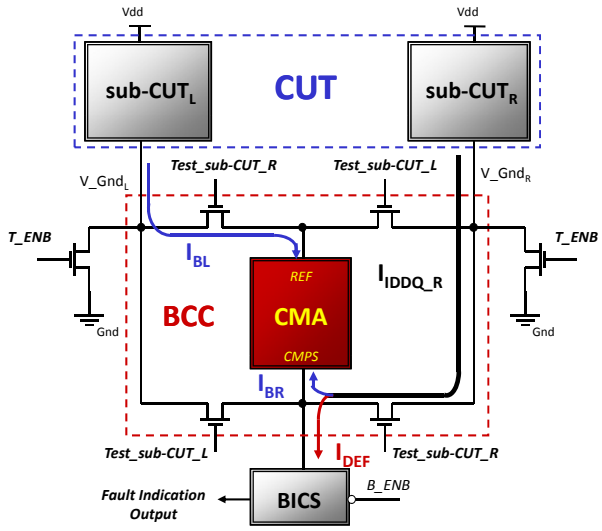


$$I_B = I_{CMP} = \beta I_{Ref}$$

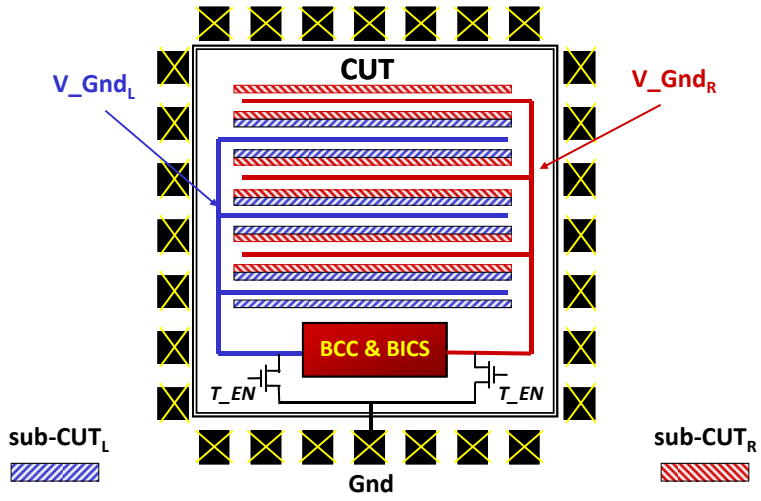
Process and Temperature Dependent BCC



Background Compensation I_{DDQ} Testing



Circuit Power Partition

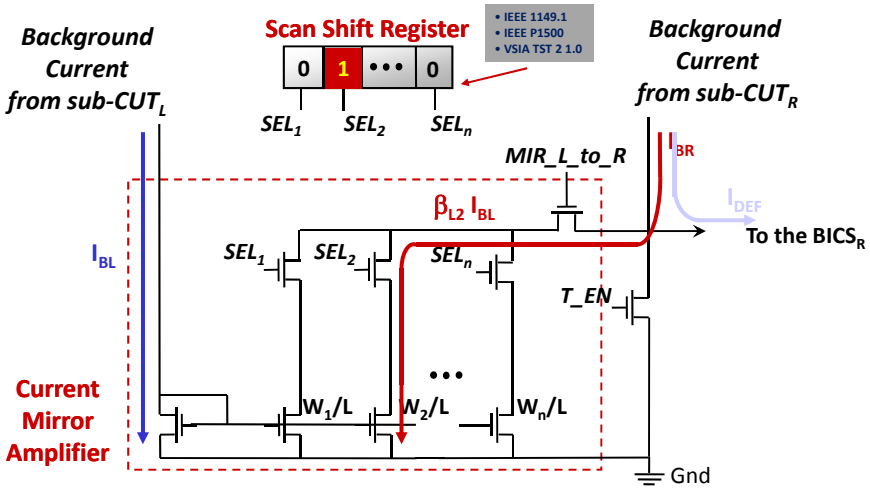


I_{DDQ} Dependence on the Input Vector

There is a strong dependence of the I_{DDQ} current to the applied input vector

Solution: The use of a CMA with programmable current gain!

- ✓ **Proper selection of test vectors (through simulations)**
- ✓ **Grouping of test vectors with neighboring I_{DDQ} currents**

The number of test vectors for I_{DDQ} testing is too small !!

Multiple Current Sink BCC