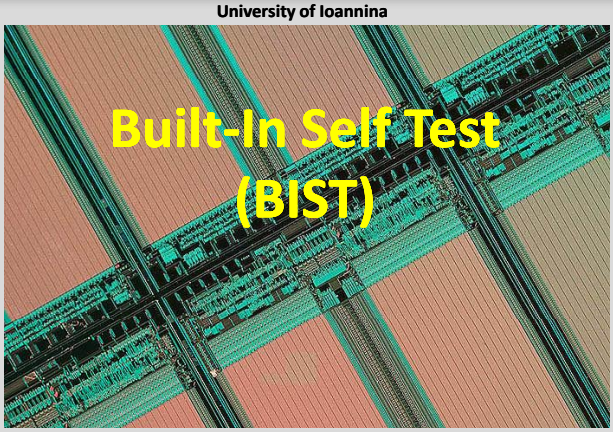
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

University of Ioannina



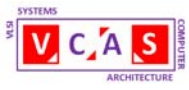
Dept. of Computer Science and Engineering

Y. Tsiatouhas

CMOS Integrated Circuit Design Techniques

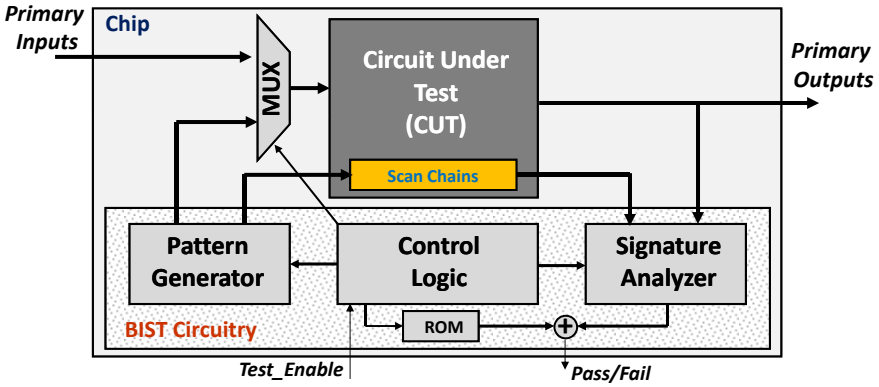
Overview

1. ***Embedded test pattern generation***
2. ***Output response analysis***
3. ***Linear feedback shift registers (LFSRs)***
4. ***Circular BIST***
5. ***Built-in logic blocks observer (BILBO)***
6. ***The STAMPS architecture***
7. ***LFSR reseeding and bit-fixing***
8. ***Design for Diagnosis***



VLSI Systems
and Computer Architecture Lab

A General Built-In Self Test (BIST) Scheme

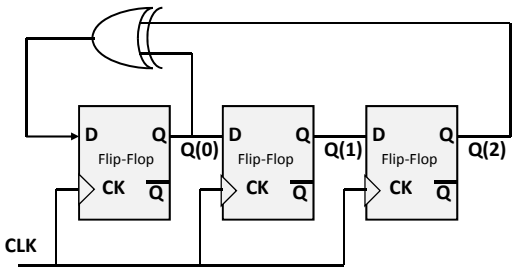


In *Built-In Self Test* schemes the test vectors are generated inside the chip and they are applied to the CUT under the control of the BIST controller. The CUT responses are compacted by the signature analyzer and the final value (*signature*), after test completion, is compared with the expected signature. In case of discrepancy the CUT is characterized as defective. A proper signal (*Pass/Fail*) is activated to indicate a possible fault detection.

Pseudorandom Pattern Generation

Linear Feedback Shift Registers - LFSRs

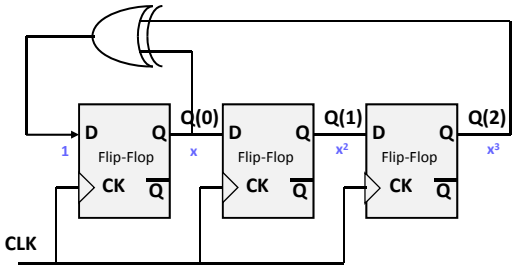
- An a LFSR acts as a pseudorandom pattern generator



Step/Cycle	Q[2...0]
0	111
1	110
2	101
3	010
4	100
5	001
6	011
7	111 repetition!

The Linear Feedback Shift Register

- An LFSR is fully described by its characteristic polynomial.
- An LFSR with characteristic polynomial of N-degree is capable to generate a maximal length cycle 2^N-1 if its polynomial is a primitive polynomial.
- An N-degree polynomial is primitive if it cannot be factored and it is divisible only by itself and 1, and it divides evenly the x^k+1 polynomial only when for the integer k stands that $k=2^N-1$ but not when $k<2^N-1$.



$P(x) = 1 \cdot x^3 + 0 \cdot x^2 + 1 \cdot x + 1 = x^3 + x + 1$

Step	Q[2]	Q[1]	Q[0]
0	1	1	1
1	1	1	0
2	1	0	1
3	0	1	0
4	1	0	0
5	0	0	1
6	0	1	1
7	1	1	1

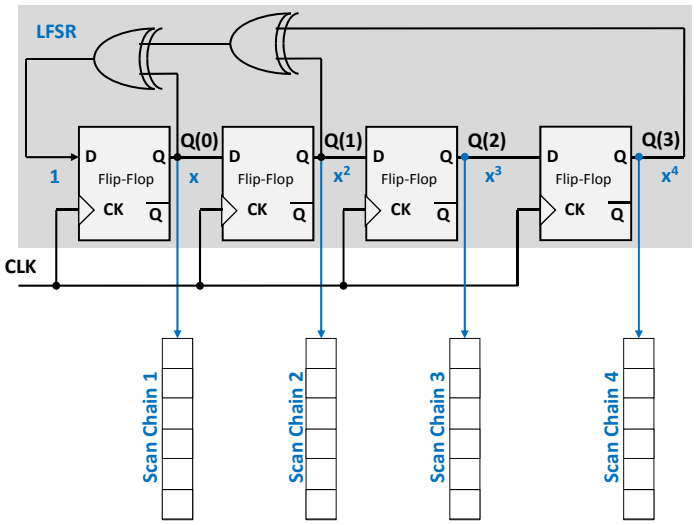
LFSR Properties

- The maximal length cycle of an LFSR with a primitive characteristic polynomial is 2^N-1.
- In a maximal length cycle "1" appears N+1 times while "0" appears N times.
- The sequence obtained at any stage j of the LFSR is one clock cycle delayed with respect to the sequence at stage j–1.

Since the generated patterns by an LFSR have a predetermined distribution of grouping bits and the sequences from different stages are self-correlated (pseudorandom patterns), some faults may be undetectable when this sequence of patterns is applied.
These faults are called: random pattern resistant (RPR) faults.

LFSR in a Typical Test Configuration

$P(x)=x^4+x^2+x+1$



Signature Analysis

The most common signature analysis technique is the sequential compaction of the CUT responses and the comparison of the final result (*signature*) with the expected one. The latter is derived by simulations on the CUT.
Usually, an LFSR is exploited for the response compaction. At the end of this operation the LFSR's contents is the *signature of the circuit*.

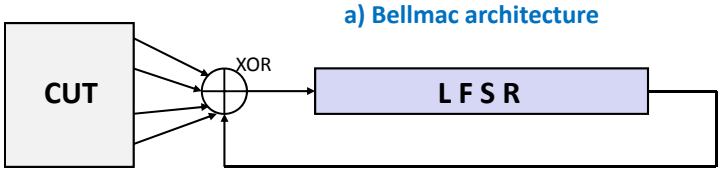
A faulty circuit is expected to provide a different signature than this of a fault free circuit.

Since response compaction may result in information loss, it is possible a faulty circuit to provide a signature identical to the expected one [the fault escapes detection (*test escape*) and the CUT is characterized as fault free]. This type of information loss is called *aliasing*.

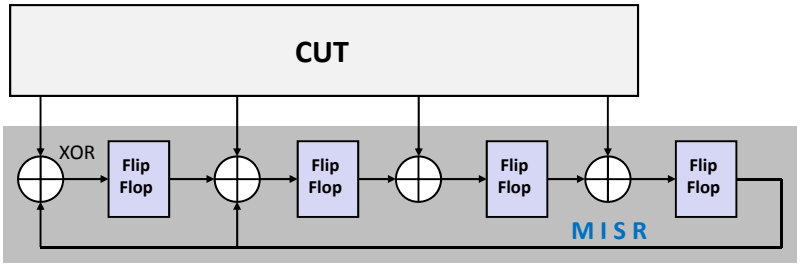
The probability of aliasing using an LFSR of N stages is: $P_a=2^{-N}$

Output Response Compaction

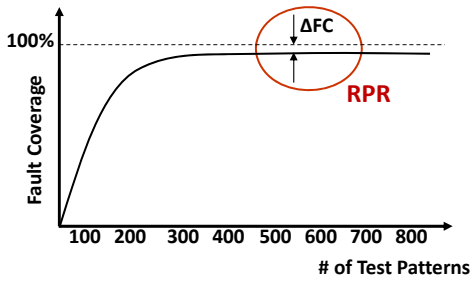
a) Bellmac architecture



b) Use of Multiple Input Shift Register - MISR



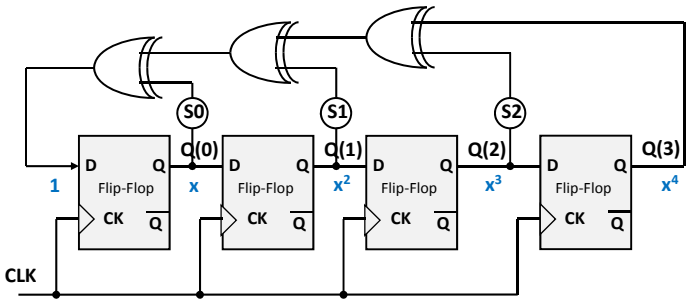
Random Pattern Resistant Faults



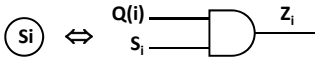
Random Pattern Resistant (RPR) Fault Alleviation Techniques

- Weighted pseudorandom pattern generation
- Aliasing reduction (e.g. multiple LFSR or MISR, collect multiple signatures)
- LFSR reseeding
- Multiple polynomial LFSR (reconfigurable LFSRs)
- Use of extra deterministic tests stored in a ROM (bit-fixing or bit-flipping)

Reconfigurable LFSR (I)



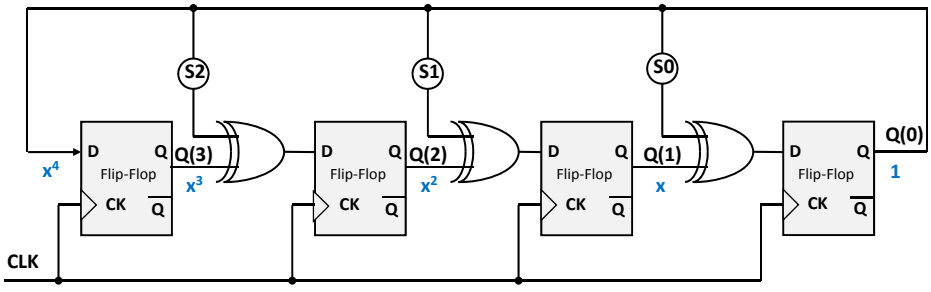
Multiple Polynomial LFSR
(Reconfigurable LFSR)



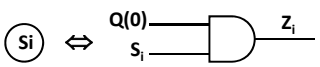
S_i	Z_i	Mode
0	0	Inactive
1	Q(i)	Active

Standard Configuration

Reconfigurable LFSR (II)



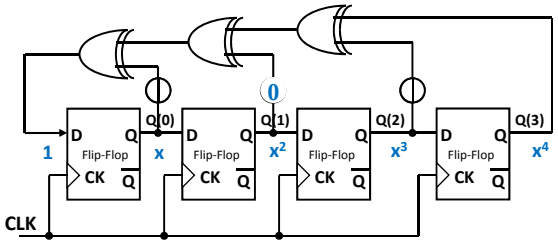
Multiple Polynomial LFSR
(Reconfigurable LFSR)



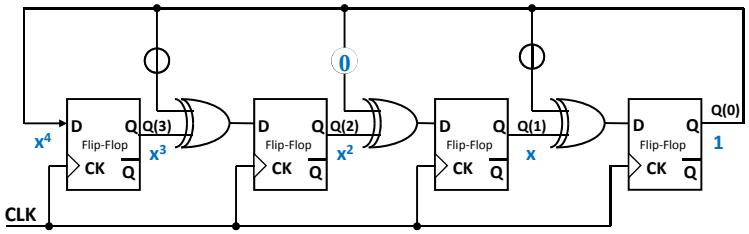
S_i	Z_i	Mode
0	0	Inactive
1	Q_0	Active

Modular Configuration

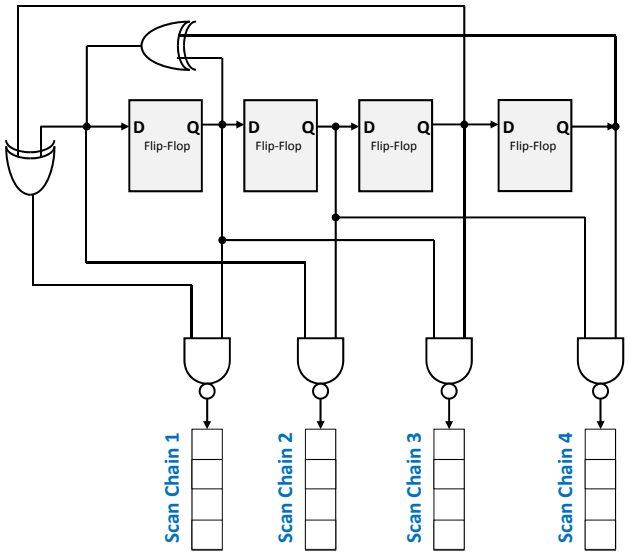
Equivalent LFSR Designs



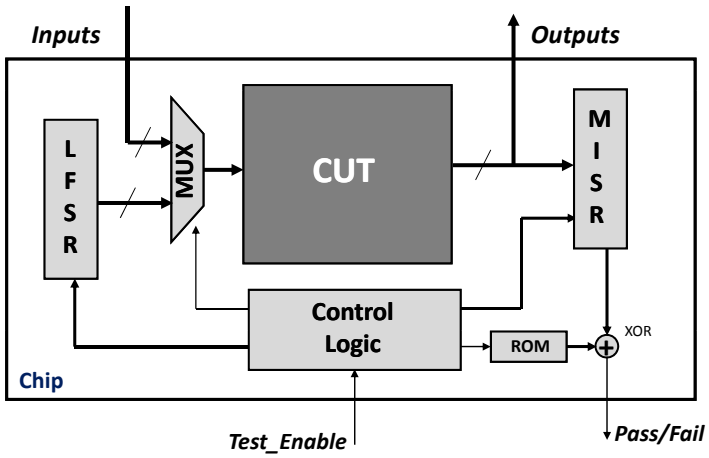
$P(x)=x^4+x^3+x+1$



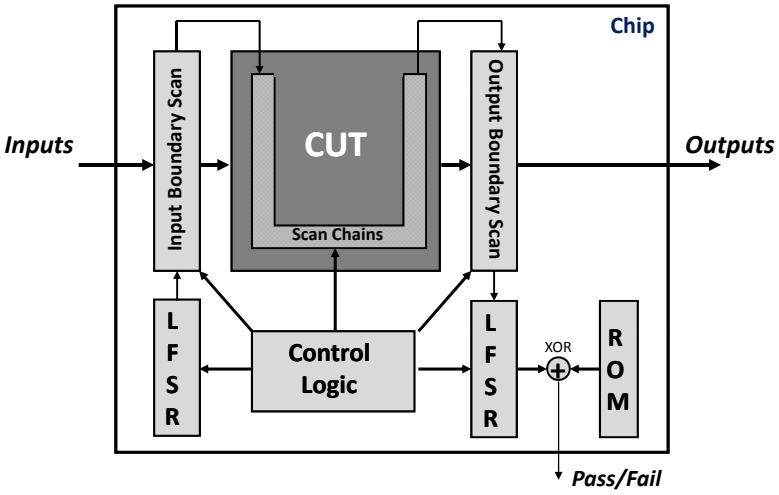
Weighted LFSR



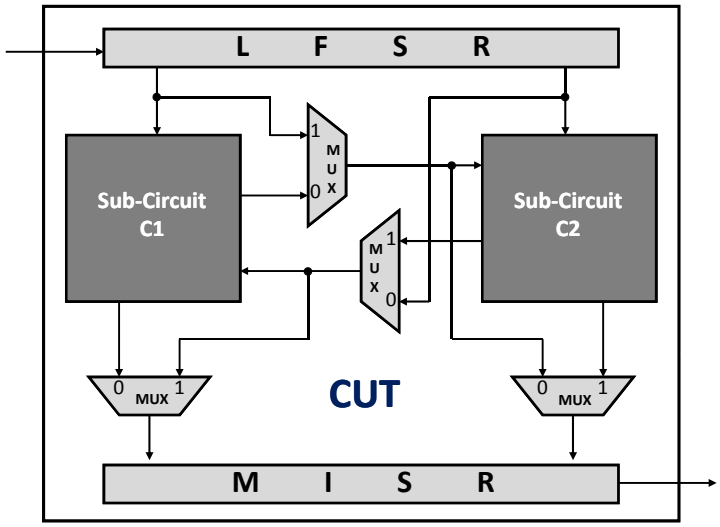
Basic BIST Architectures (I)



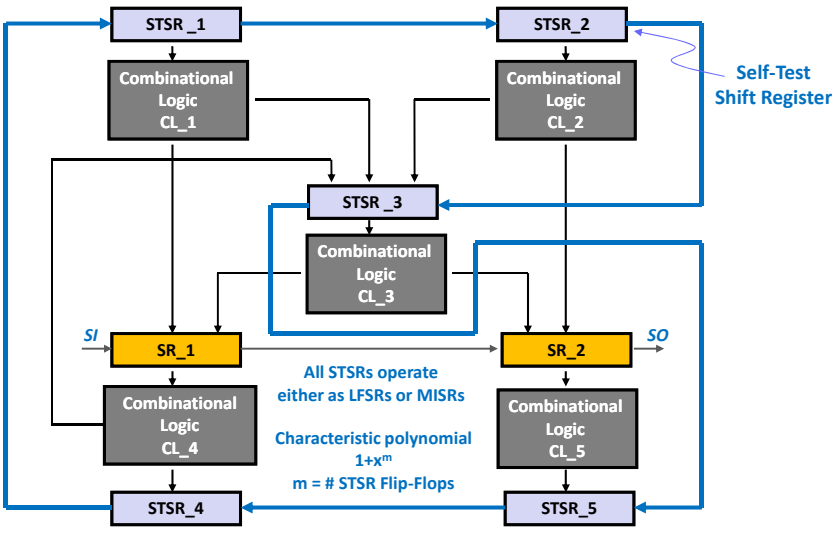
Basic BIST Architectures (II)



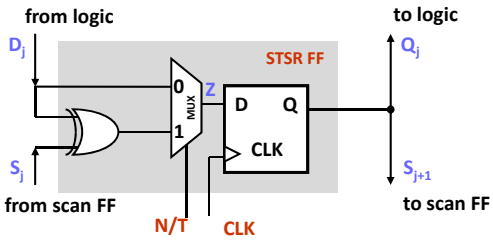
Partitioning – Autonomous BIST



Circular BIST



Circular BIST Flip-Flop

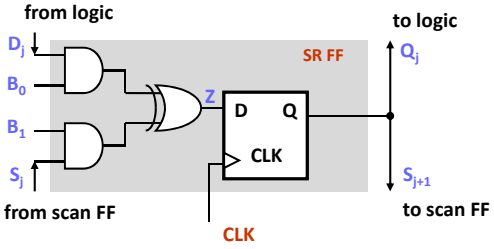


STSR Flip-Flop

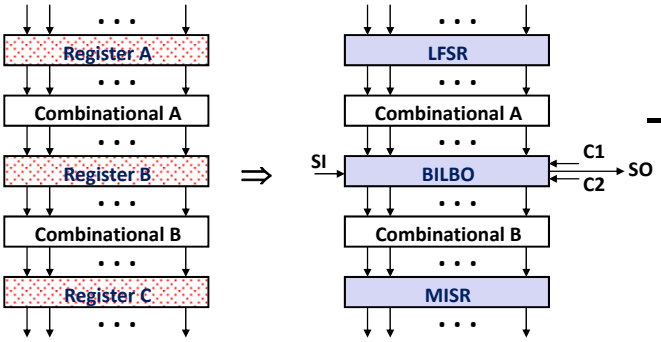
N/T	Z	Mode
0	D_j	Normal
1	$S_j \oplus D_j$	Test (LFSR-MISR)

SR Flip-Flop

B_0	B_1	Z	Mode
0	0	0	Reset
0	1	S_j	Scan
1	0	D_j	Normal
1	1	$S_j \oplus D_j$	Test (LFSR-MISR)

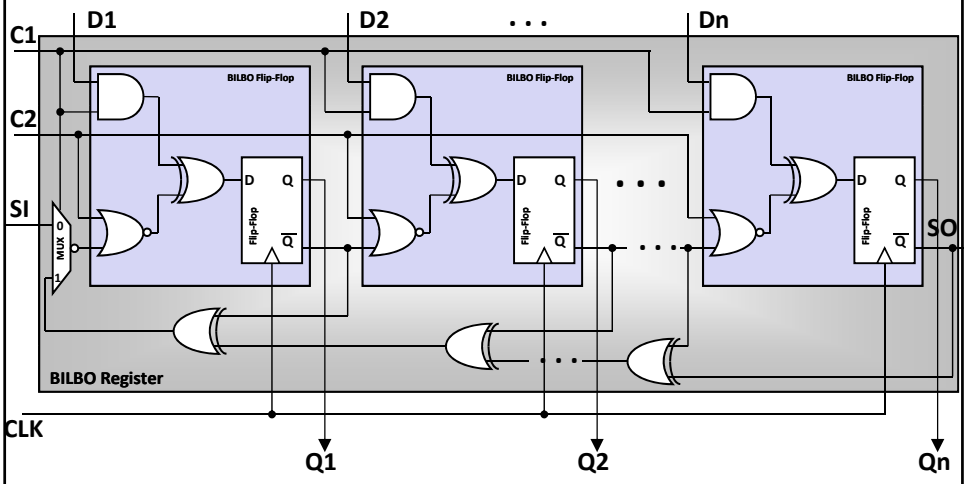


Built-In Logic Blocks Observer - BILBO

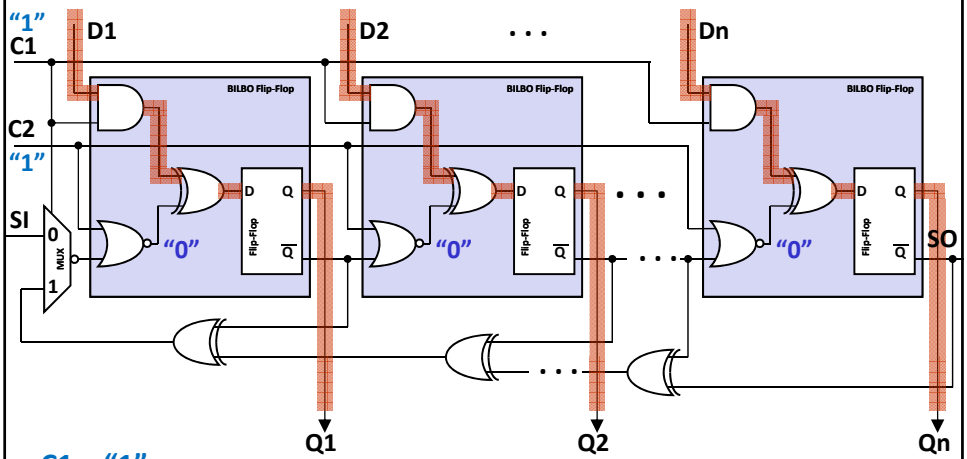


C1	C2	Mode
0	0	Scan
1	0	LFSR + MISR
1	1	Normal

BILBO Register Structure



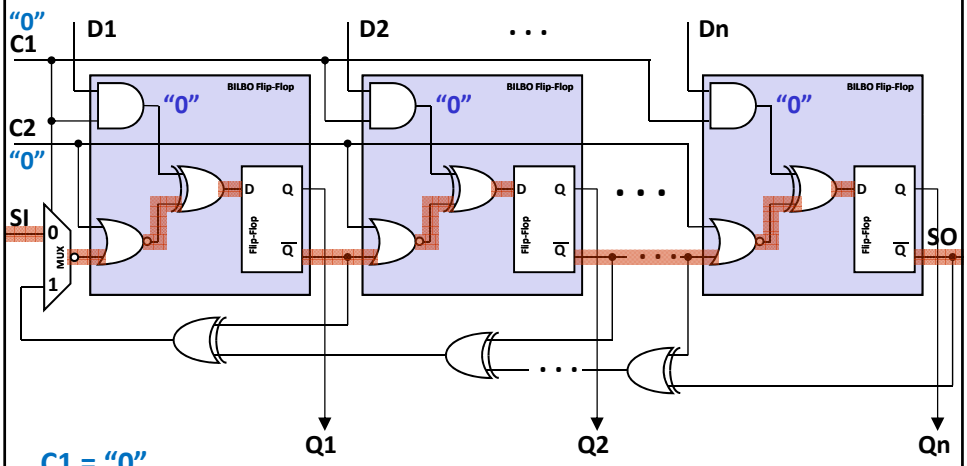
BILBO – Normal Mode



C1 = "1"

C2 = "1"

BILBO – Scan Operation Mode

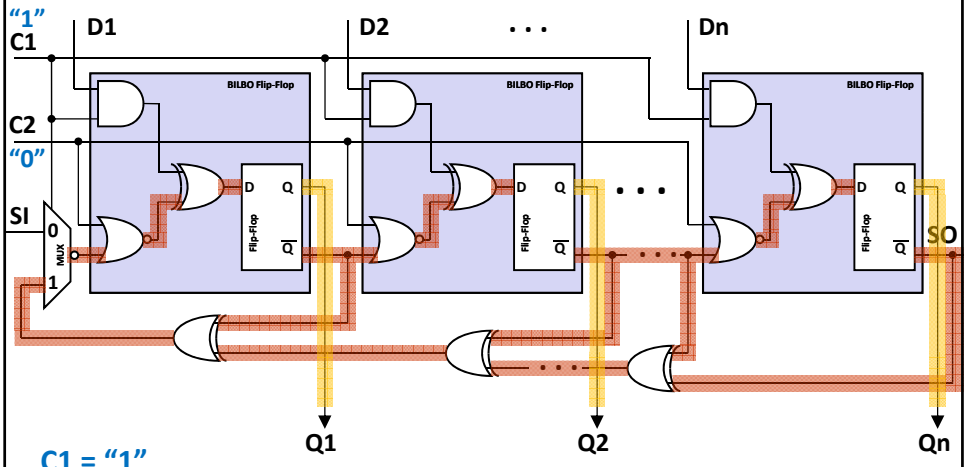


C1 = "0"

C2 = "0"

BILBO – LFSR Operation Mode

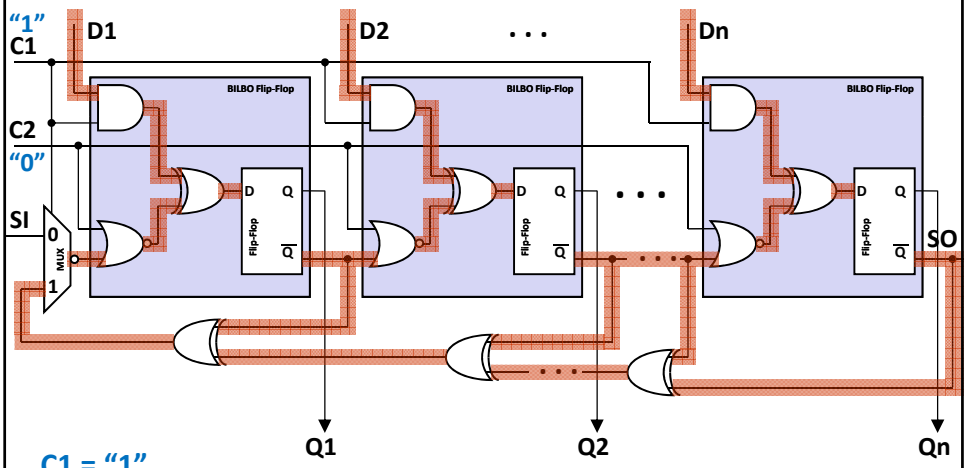
Constant Values



C1 = "1"

C2 = "0"

BILBO – MISR Operation Mode

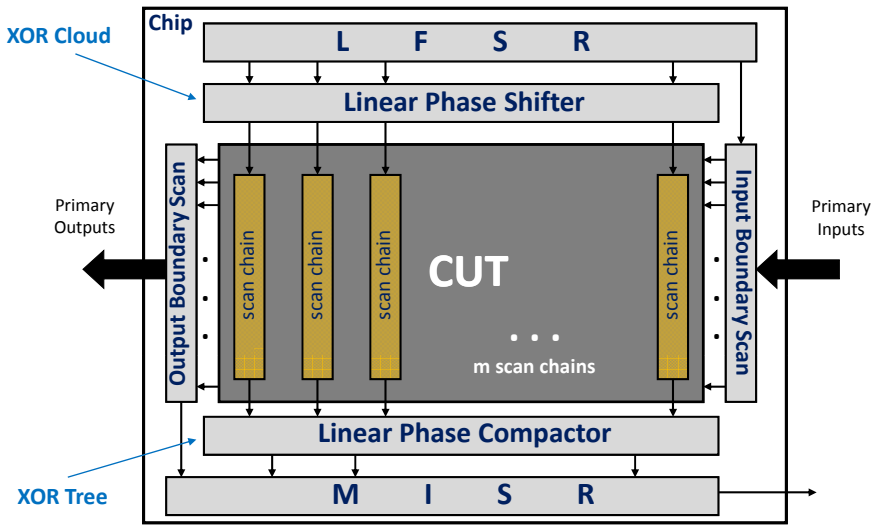


C1 = "1"

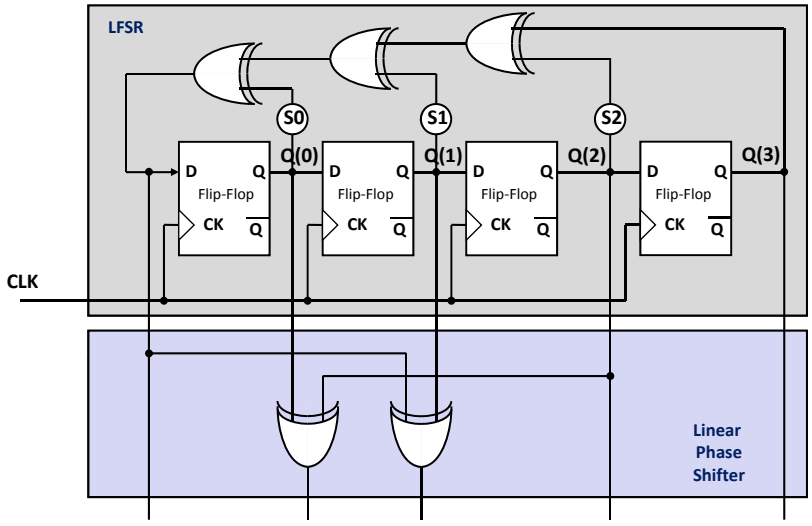
C2 = "0"

The STUMPS Architecture

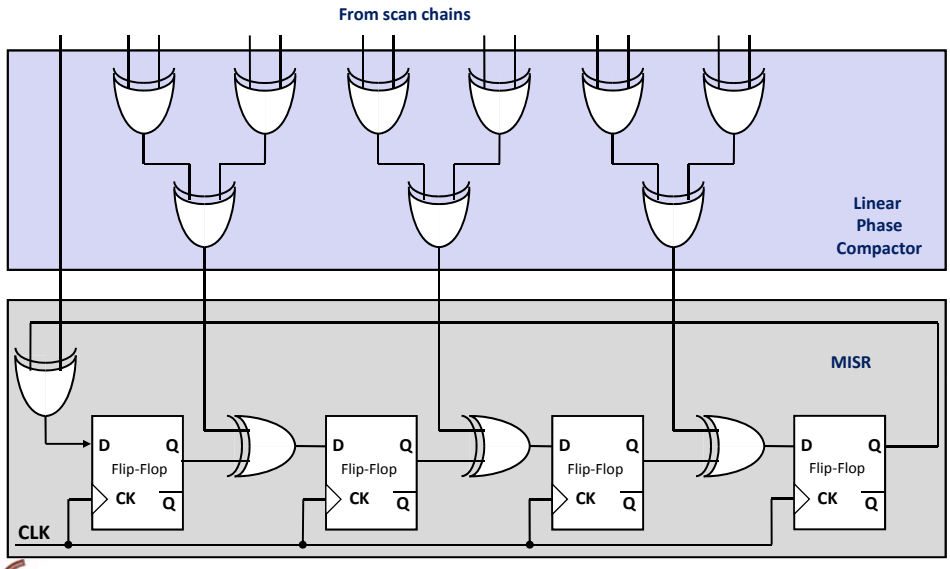
Self-Test Using MISR and a Parallel Shift Register Sequence Generator



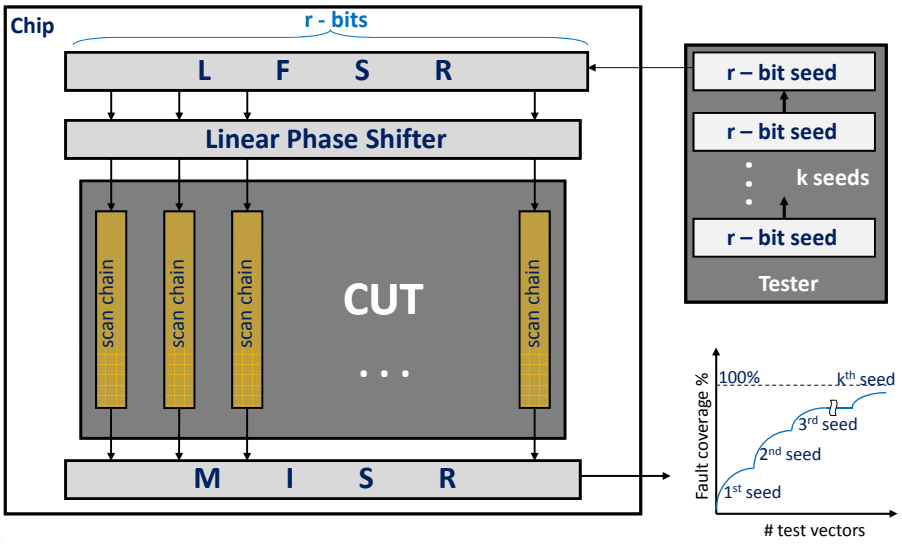
Linear Phase Shifter



Linear Phase Compactor

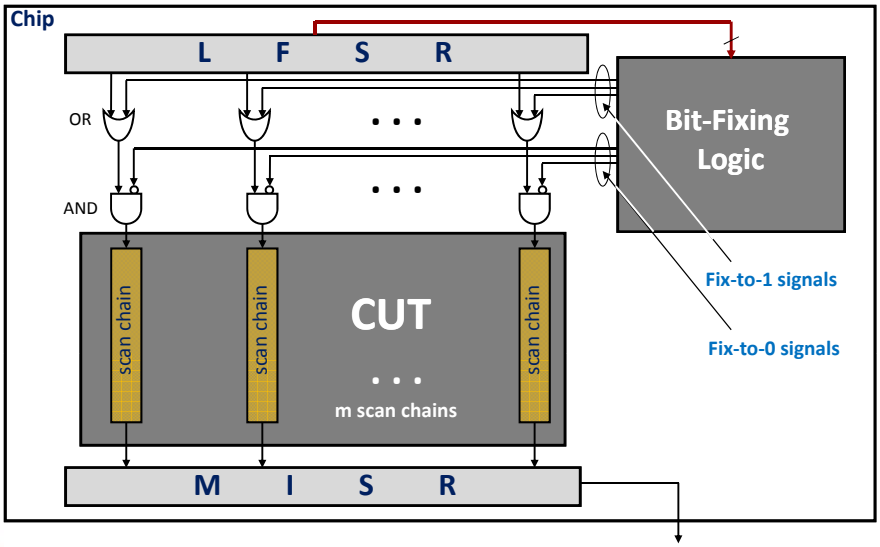


LFSR Reseeding



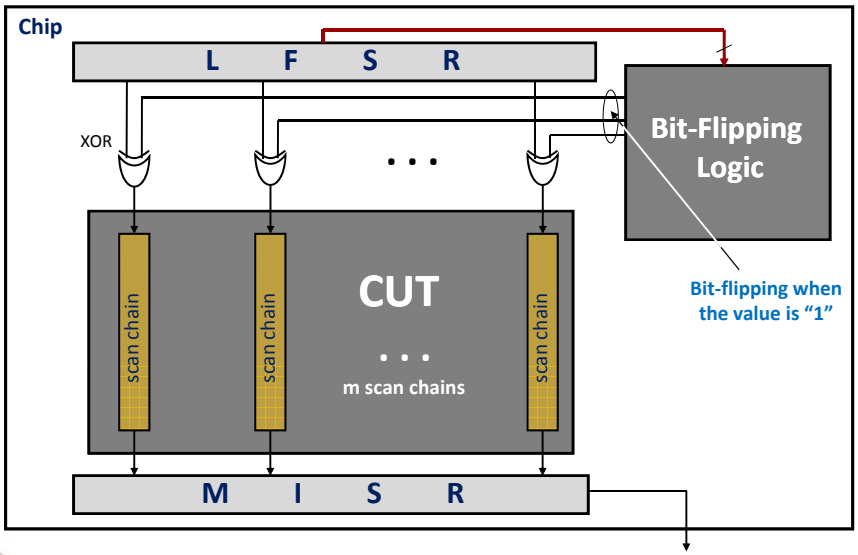
LFSR and Bit-Fixing

Embedding Deterministic Patterns



LFSR and Bit-Flipping

Embedding Deterministic Patterns



Design for Diagnosis

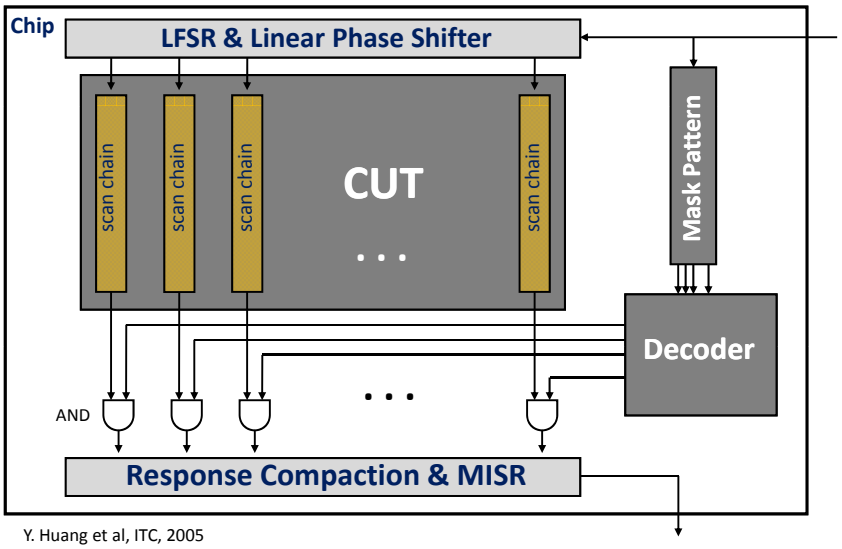
As *Diagnosis* we define those operations that are performed in order to locate defects in an integrated circuit. This information is used to improve the manufacturing process or the quality of the design and consequently to increase the yield.

Design for testability techniques may increase the difficulty to diagnose faults. A main problem comes from the scan chain output compaction schemes.

Hardware assisted, software assisted (the inject and evaluate paradigm) and signal-profiling based techniques are exploited for fault diagnosis.

In all diagnosis techniques, special diagnosis vectors (or the existing test vectors) are used for defect location.

Compressed Pattern Diagnosis



Y. Huang et al, ITC, 2005

References

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- "**Essentials of Electronic Testing: for Digital, Memory and Mixed-Signal VLSI Circuits**", M. Bushnell and V. Agrawal, *Kluwer Academic Publishers*, 2000.
- "**Digital Systems Testing and Testable Design**", M. Abramovici, M. Breuer and A. Friedman, *Computer Science Press*, 1990.
- "**Bit-Fixing in Pseudorandom Sequences for Scan BIST**", N. Touba and J. McCluskey, IEEE Tran. on CAD of Integrated Circuits and Systems, vol. 20, no.4, pp. 546-555, 2001.
- "**System-on-Chip Test Architectures**", L-T Wang, C. Stroud and N. Touba, Morgan-Kaufmann, 2008.