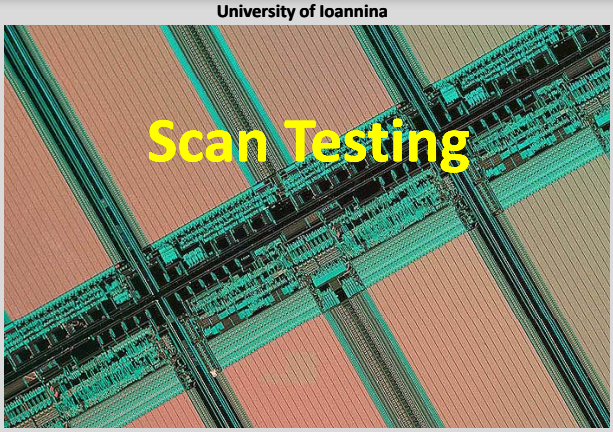
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

University of Ioannina



Dept. of Computer Science and Engineering

Y. Tsiatouhas

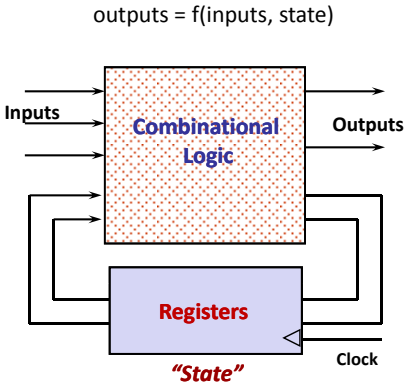
CMOS Integrated Circuit Design Techniques

Overview

VLSI Systems
and Computer Architecture Lab

1. *Scan testing: design and application*
2. *At speed testing*
3. *The scan-set design technique*
4. *Scan testing power issues*
5. *The scan-hold design technique*
6. *Level sensitive scan design*
7. *Broadcast and Illinois scan design*

Sequential Circuits Testing

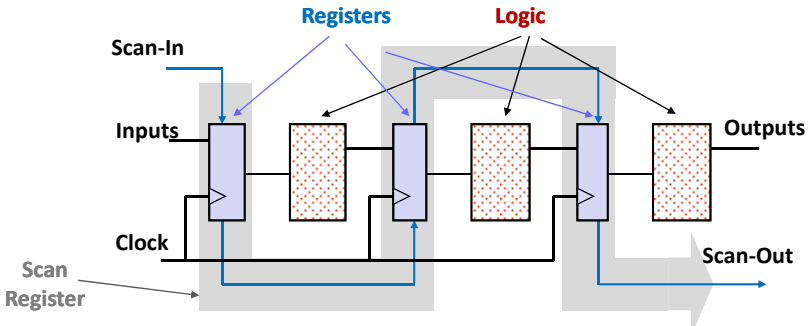


In sequential circuits the initial state (register's values) is not by default known. Consequently, the sensitization of faults and the propagation of the corresponding erroneous responses may turn to be a hard task.

A solution is to use techniques for the proper initialization of the circuit state to known values.

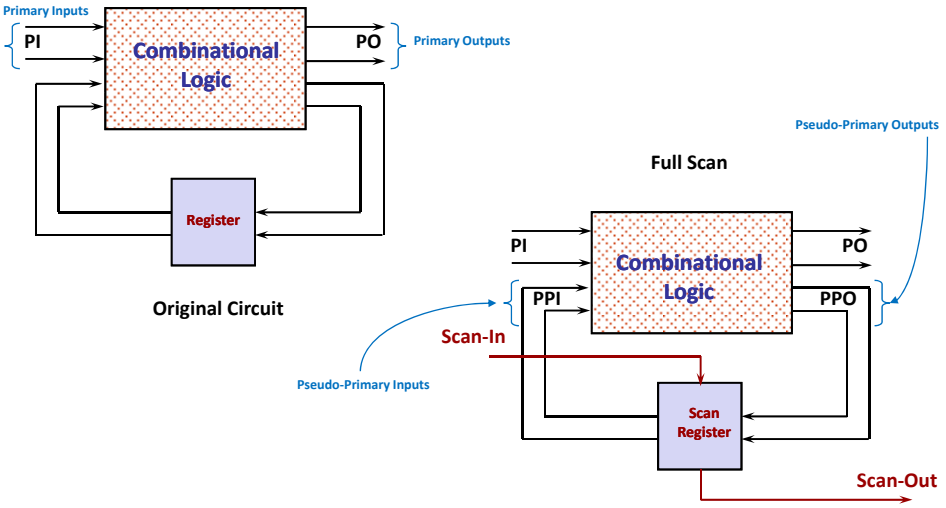
- Application of proper test vector sequences and/or the use of *Set*/*Reset* signals to setup the required state.
- Development of efficient techniques to set the initial state and observe the subsequent state after the response of the circuit.

General Scan Testing Scheme

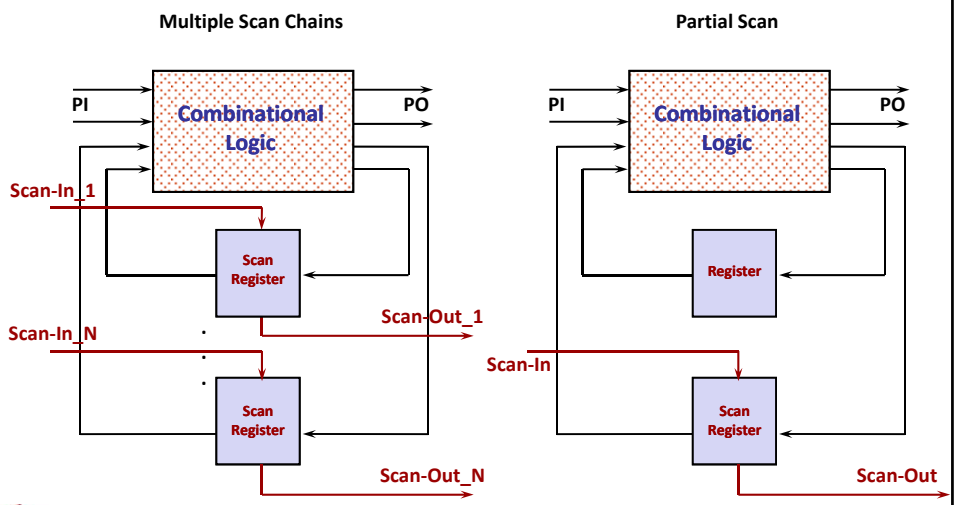


The memory elements (latches or Flip-Flops) in a design are properly connected to form a unified shift register (*scan register* or *chain*). This way the internal state of the circuit is determined (controlled) by shifting in (*scan-in*) to the scan register the required test data to be applied to the combinational logic. Moreover, the existing internal state (previous logic response) can be observed by shifting out (*scan-out*) the data stored into the scan register.

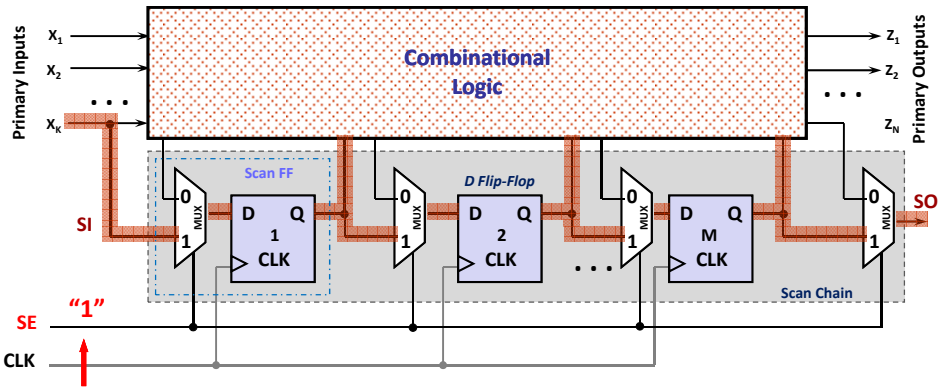
Scan Testing Design (I)



Scan Testing Design (II)

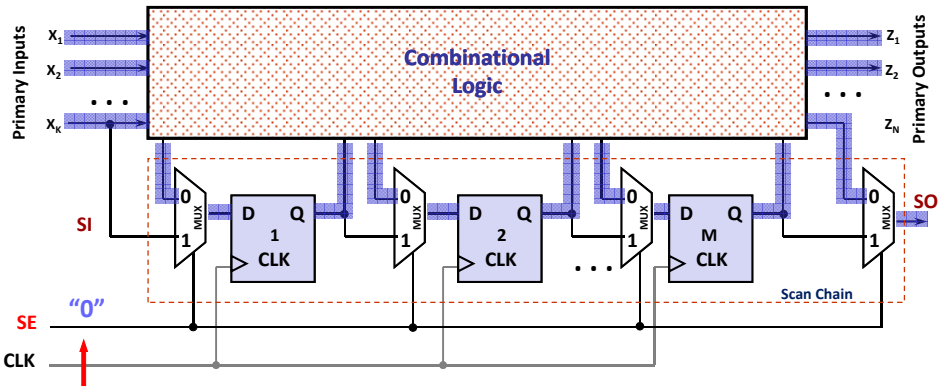


Scan Path Design (I)



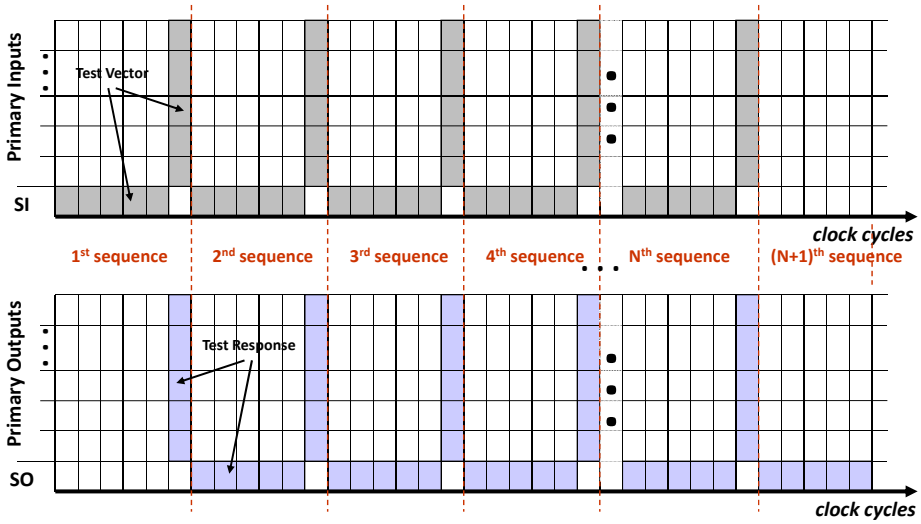
Scan Mode
SE="1"

Scan Path Design (II)



Normal Mode
SE="0"

Test Sequences During Scan Testing

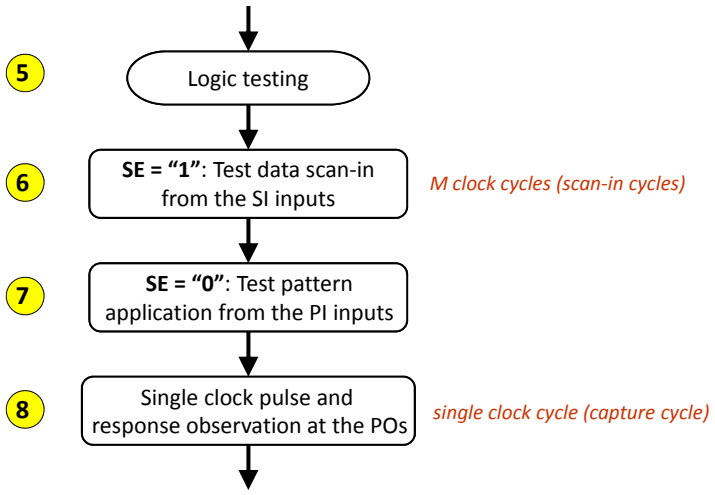


Scan Application (I)

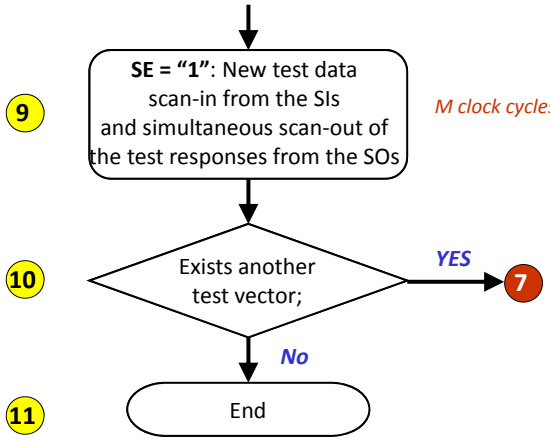
1. Scan cells testing
2. SE = "1"
3. Scan-in of alternating "0" and "1" from the SI input — *≥ M+1 clock cycles*
4. Response observation at the SO output

M = # of scan cells

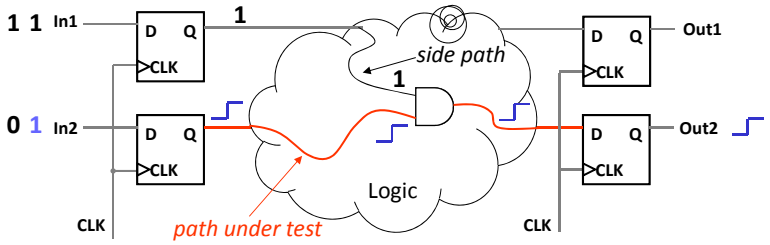
Scan Application (II)



Scan Application (III)



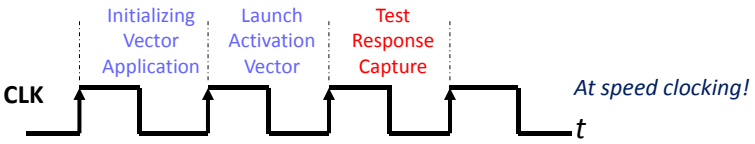
Delay Fault Testing



V1 = <10> ← Initializing test vector
V2 = <11> ← Path activation test vector

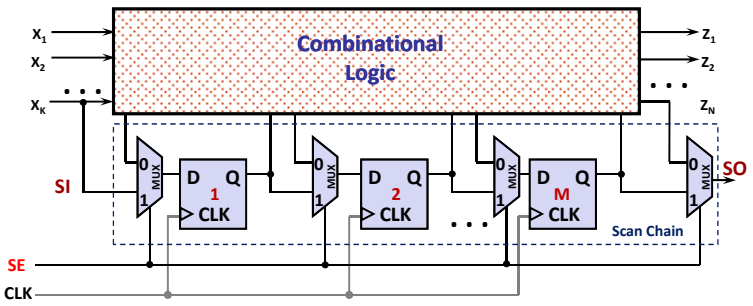
A path delay fault requires a pair of subsequent test vectors to be detected.
The first test vector initializes the circuit while the second test vector activates the path under test.

How scan testing facilities can be exploited for delay fault testing ?

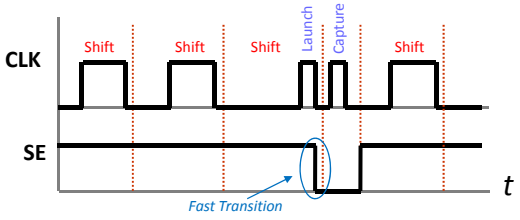


At Speed Scan Testing (I)

(Skewed-load or Launch-on-shift Technique)

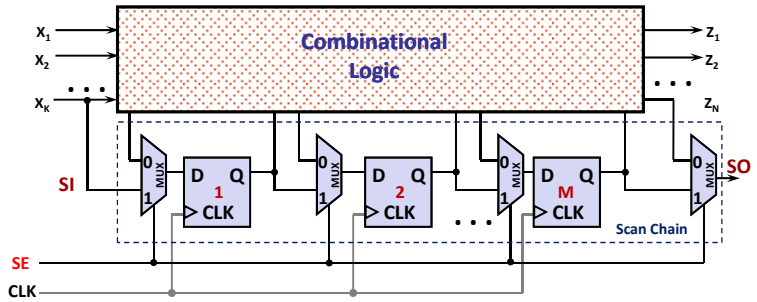


Delay fault oriented scan testing technique

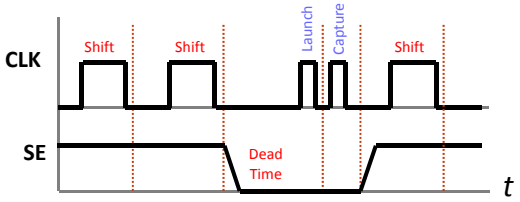


At Speed Scan Testing (II)

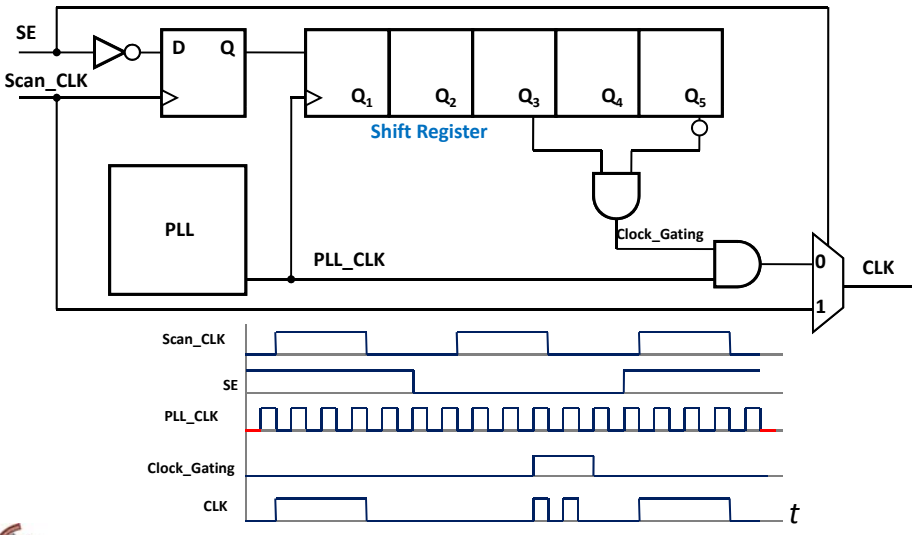
(Double Capture or Launch-on-Capture Technique)



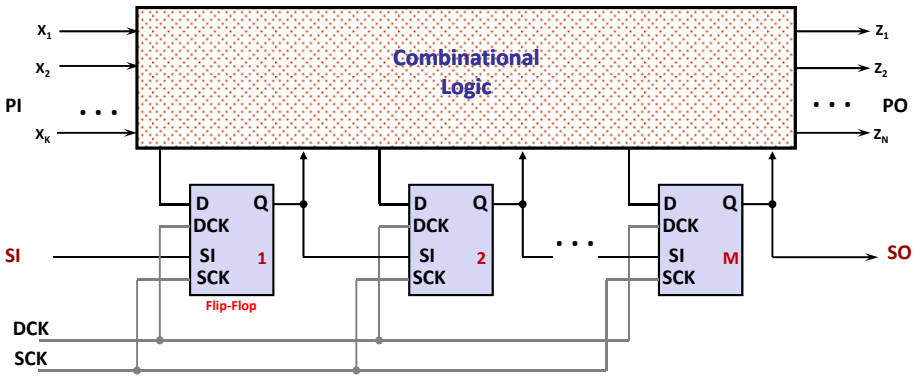
Delay fault oriented scan testing technique



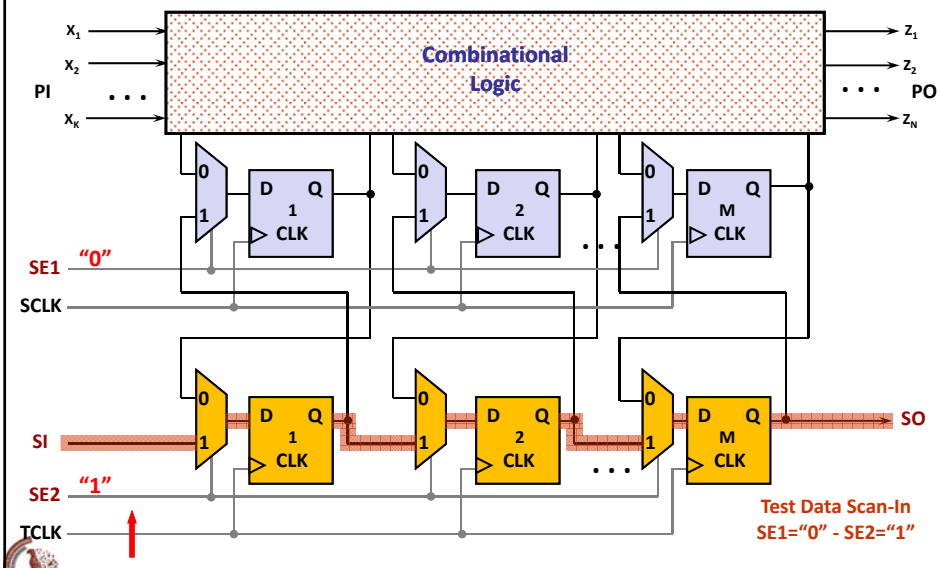
Fast Clock Pulses Generation



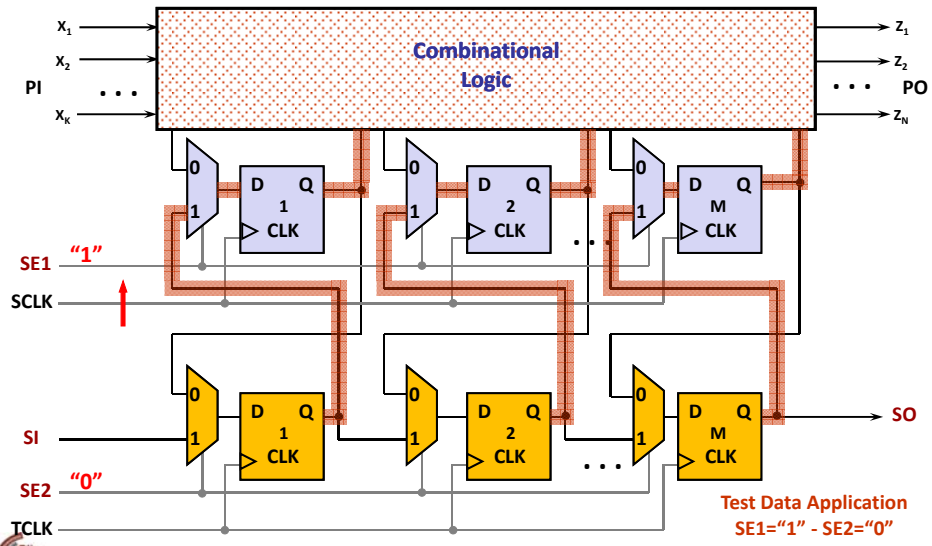
The Clocked-Scan Technique



The Scan-Set Technique (I)

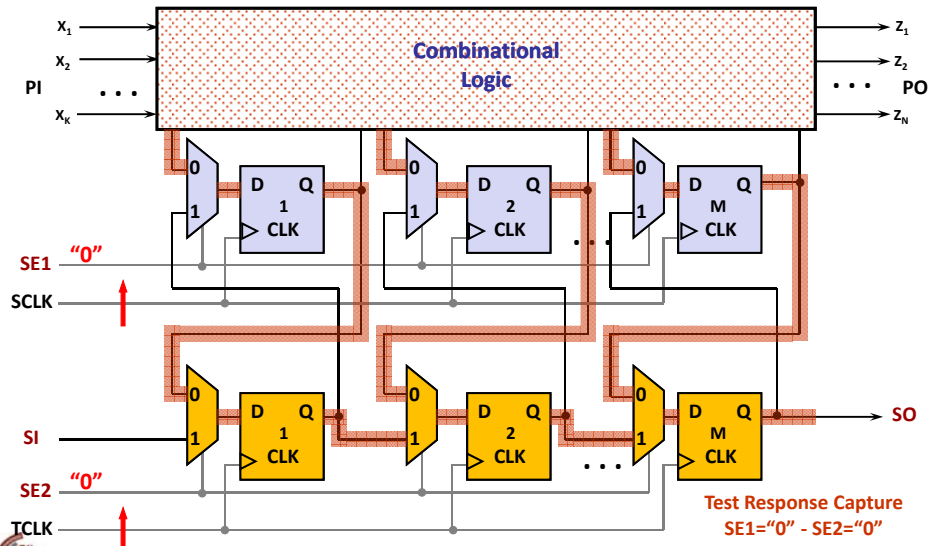


The Scan-Set Technique (II)



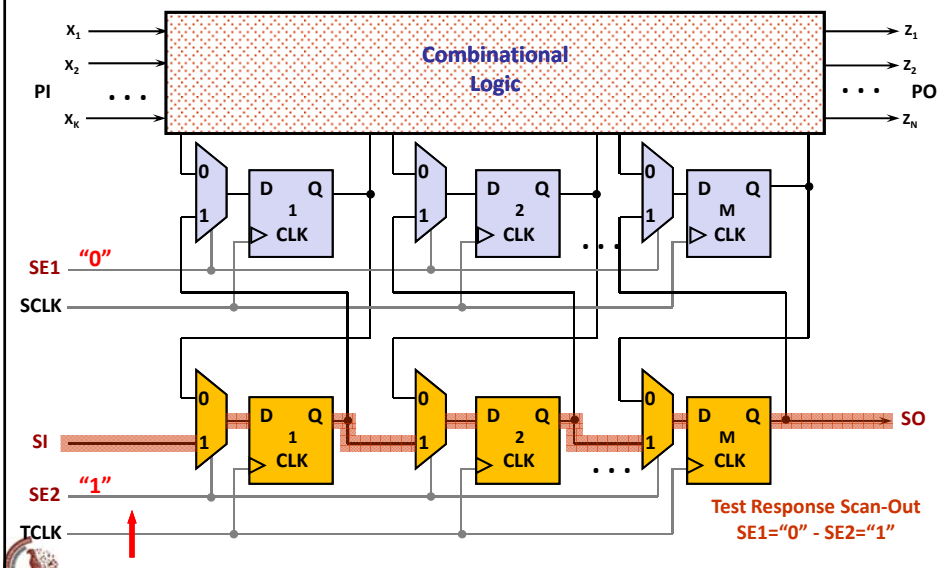
Test Data Application
SE1="1" - SE2="0"

The Scan-Set Technique (III)

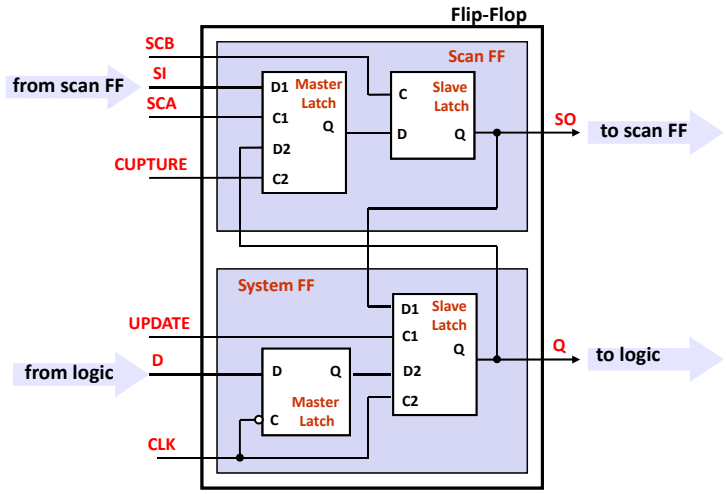


Test Response Capture
SE1="0" - SE2="0"

The Scan-Set Technique (IV)



Dual Flip-Flops Scan Architecture

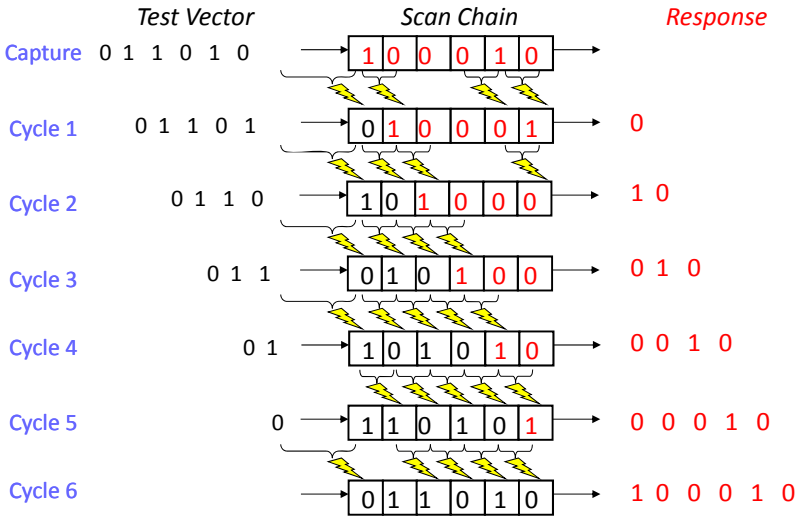


Intel

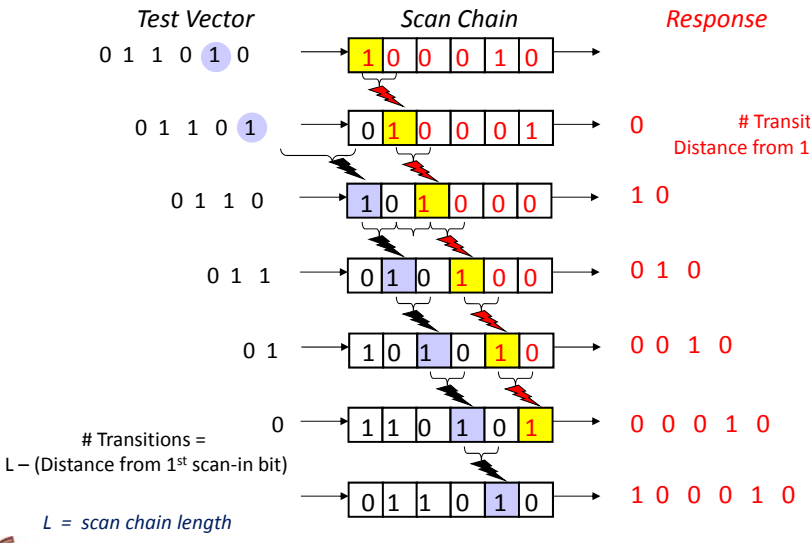
Scan Testing Impact

- Silicon area and pin count cost.
- Speed performance degradation.
- Test application time cost.
- Excess power consumption (usually outside circuit's specifications) during the scan-in/out operations and the capture of the test response in the scan chain.

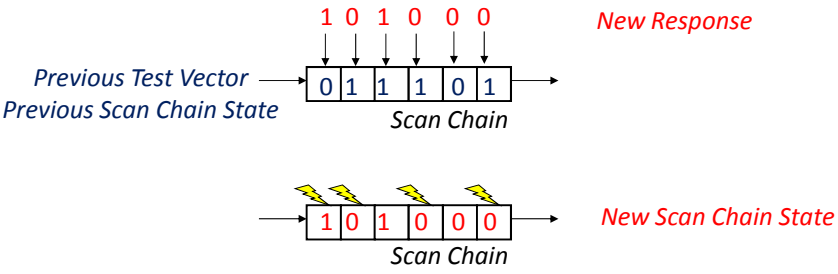
Scan Chain Shift Power Consumption (I)



Scan Chain Shift Power Consumption (II)



Scan Chain Capture Power Consumption

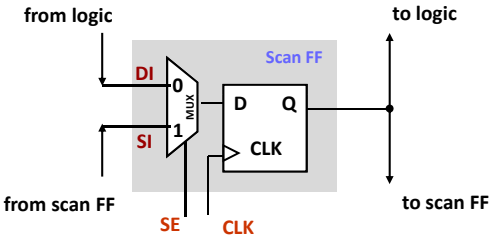


Power consumption during scan testing procedures is a major concern since it can be several times higher than this during the normal mode of operation. This can affect the reliability of the circuit under test (CUT) due to overheat and electromigration phenomena.
The excessive switching activity of the CUT during the scan operations may violate the power supply IR and Ldi/dt drop limitations and increase the probability of noise induced test failures. In addition, the elevated temperature can degrade the speed performance of the CUT and result to erroneous test responses that will invalidate the testing process and lead to yield loss.

X-bit Assignment

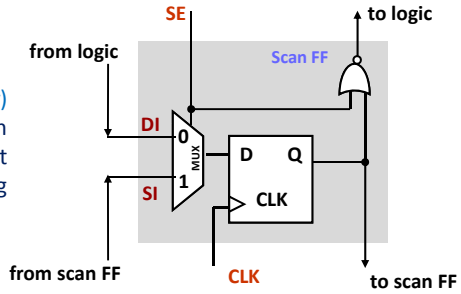
- A large number of bits in a test cube that is generated by an ATPG tool are don't care bits (X-bits).
- In order to apply a test cube for circuit testing, specific values must be assigned to the X-bits (test vector formation). This task is called X-filling.
- The X-filling process can be oriented for shift and/or capture power reduction.

Low Power Scan

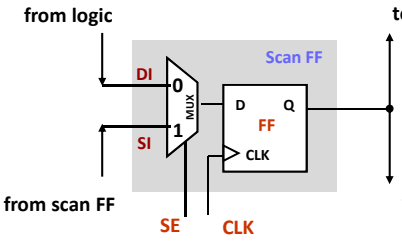


Original Topology

Use of *Data Gating* (*φραγμός δεδομένων*) techniques at the output of the scan cells in order to eliminate the signal transitions at the inputs of the combinational logic during the scan-in/out operations.
Dynamic power reduction.



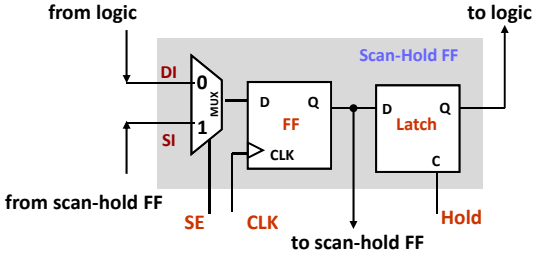
Scan-Hold Flip-Flop



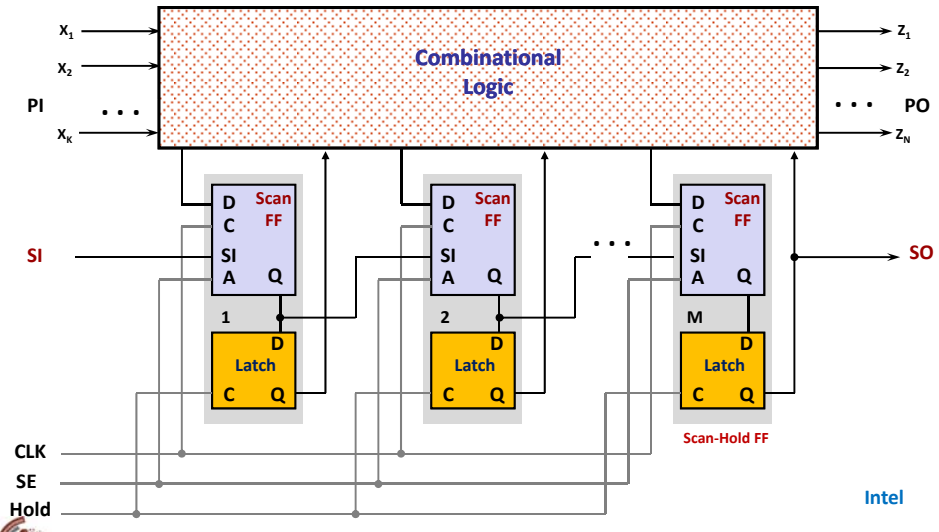
Original Topology

Delay testing oriented Flip-Flop!

+ Dynamic power reduction.

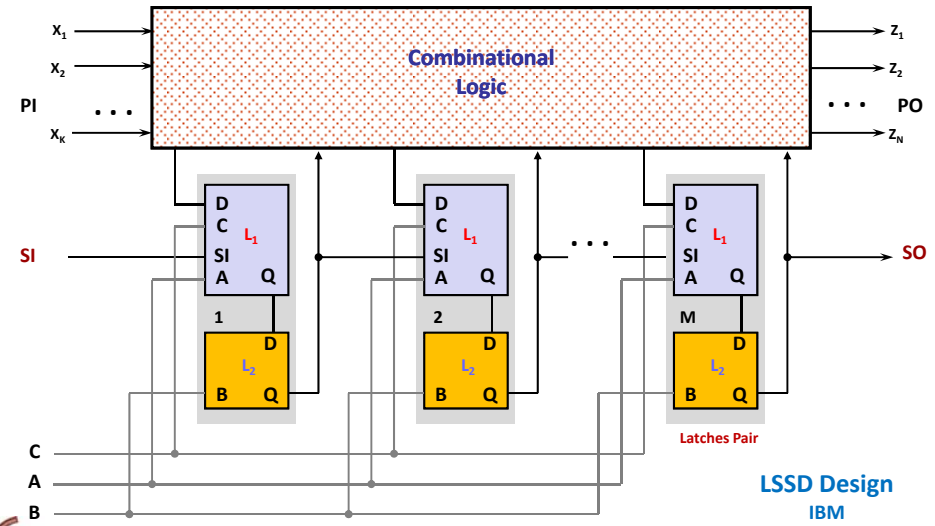


The Scan-Hold Technique

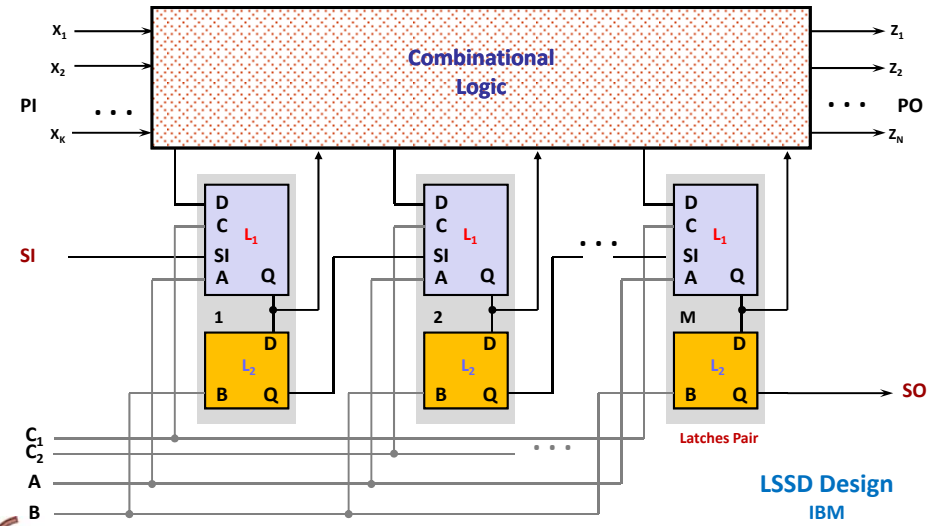


Intel

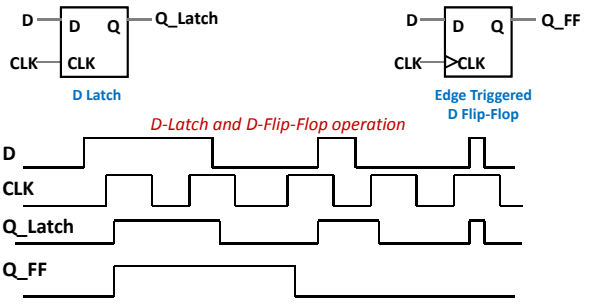
Level Sensitive Scan Design (I)

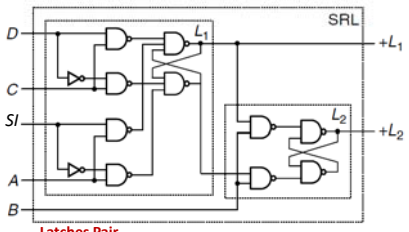


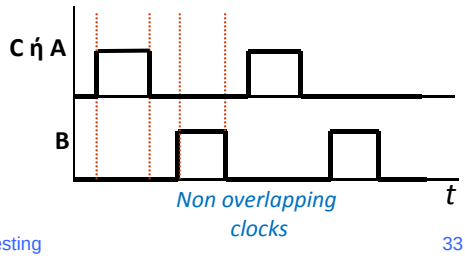
Level Sensitive Scan Design (II)



Level Sensitive Scan Design (III)



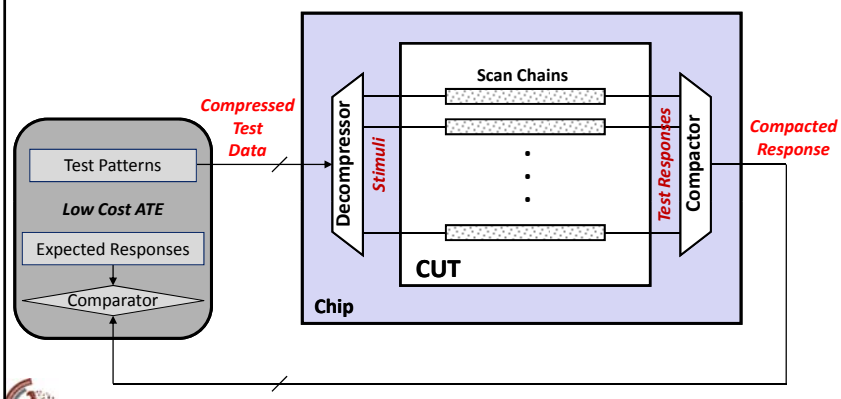




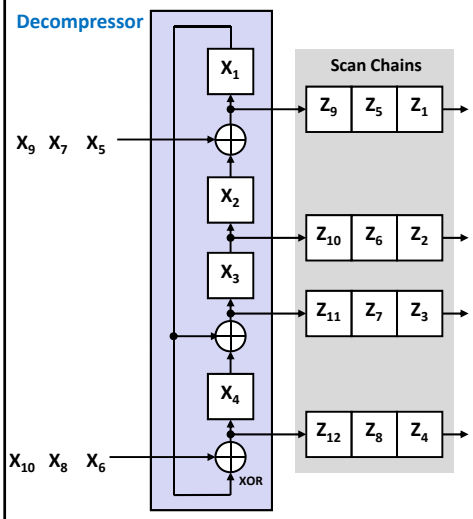
Test Data Compression

Typically, ATPG tools generate test vectors where only 1% to 5% of the bits have specified values!

On the other hand, test data volume is a major concern for the available bandwidth and the ATEs' storage capabilities.

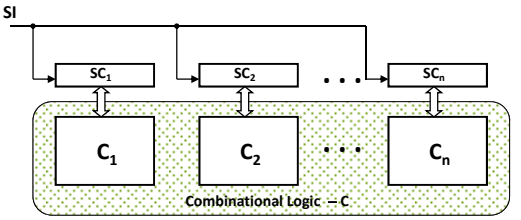


Linear Decompression

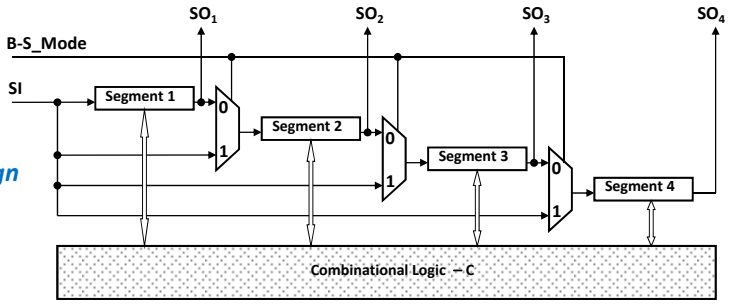


$Z_9 = X_1 \oplus X_4 \oplus X_9$	$Z_5 = X_3 \oplus X_7$	$Z_1 = X_2 \oplus X_5$
$Z_{10} = X_1 \oplus X_2 \oplus X_5 \oplus X_6$	$Z_6 = X_1 \oplus X_4$	$Z_2 = X_3$
$Z_{11} = X_2 \oplus X_3 \oplus X_5 \oplus X_7 \oplus X_8$	$Z_7 = X_1 \oplus X_2 \oplus X_5 \oplus X_6$	$Z_3 = X_1 \oplus X_4$
$Z_{12} = X_3 \oplus X_7 \oplus X_{10}$	$Z_8 = X_2 \oplus X_5 \oplus X_8$	$Z_4 = X_1 \oplus X_6$

Broadcast & Illinois Scan Design

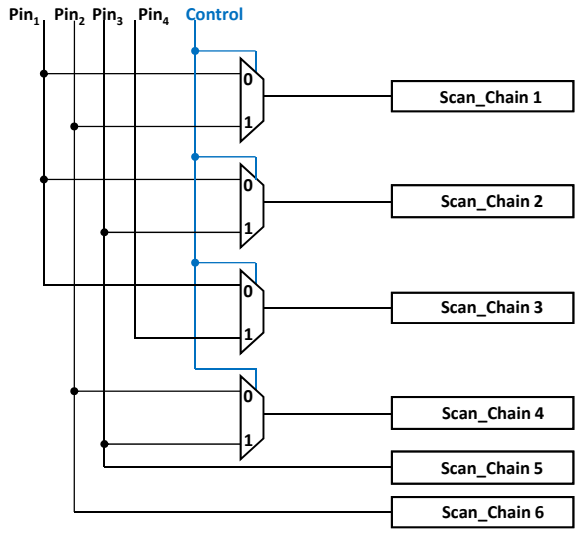


Broadcast Scan Design



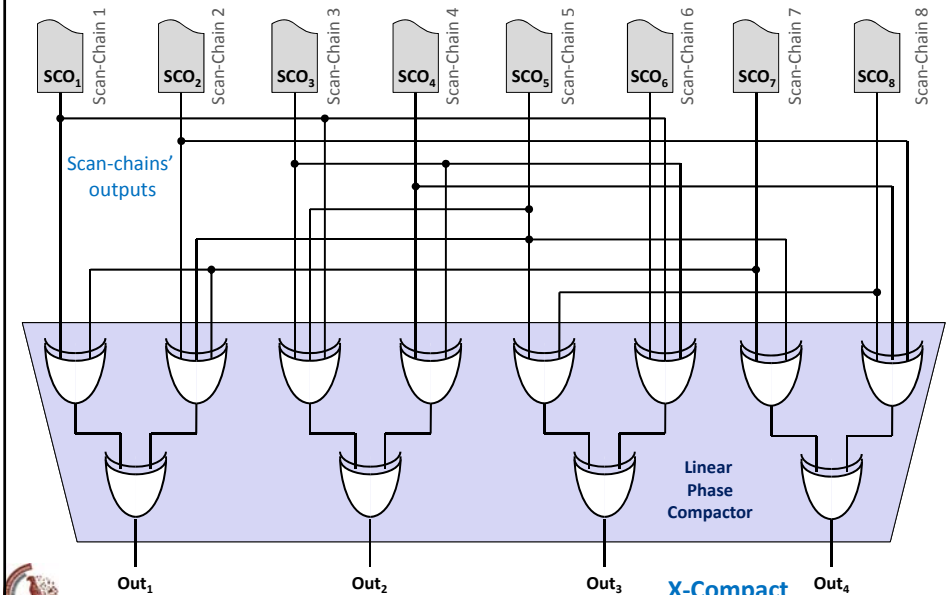
Illinois Scan Design

Reconfigurable Broadcast Scan Design



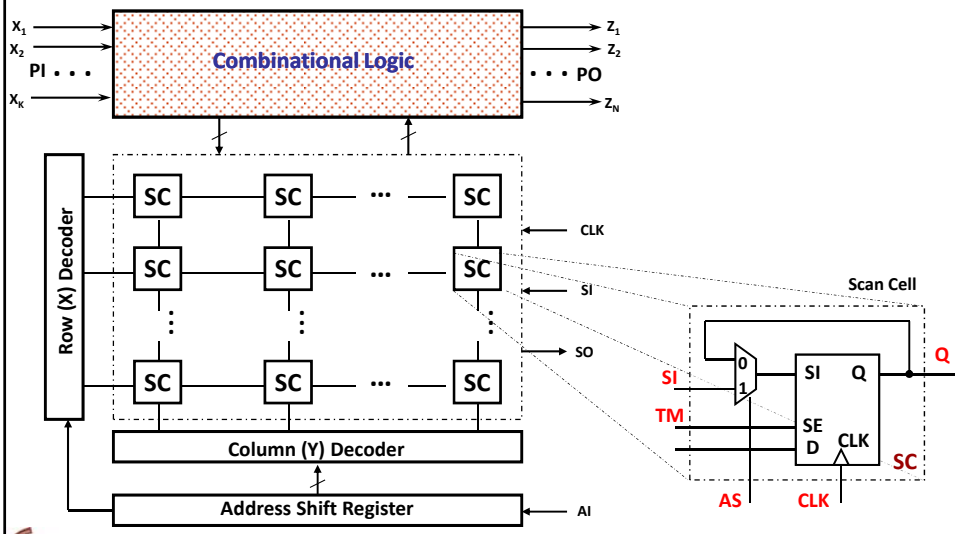
Dynamic Reconfiguration

Space Compaction



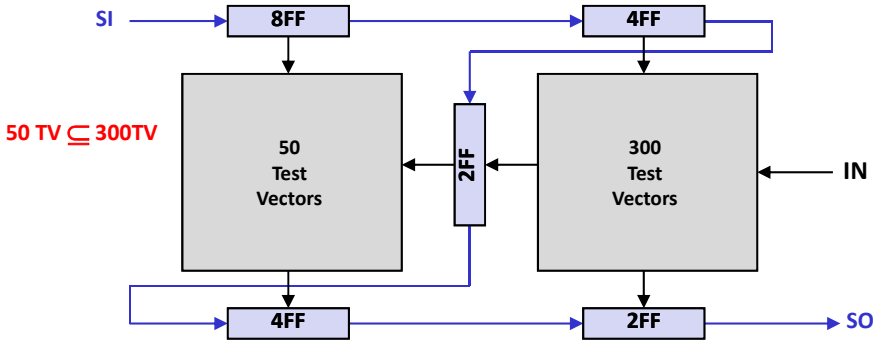
X-Compact

Random–Access Scan Design



Reordering of Scan Chain Flip-Flops (I)

Typical Scan Chain



Test Application: 300(20+1)+20 = 6320 clock cycles

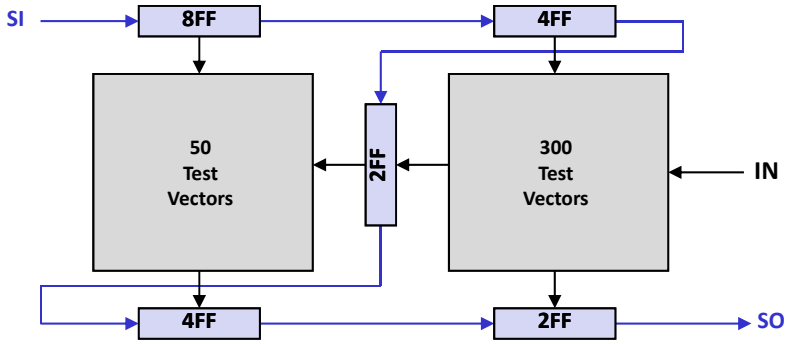
"Random" register connection

1st Alternative Test Application: 300(14+1)+8 = 4508 clock cycles

Improvement 29% !

Reordering of Scan Chain Flip-Flops (II)

2nd Alternative Scan Testing Application



Test Application: 50(14+1) = 750 clock cycles

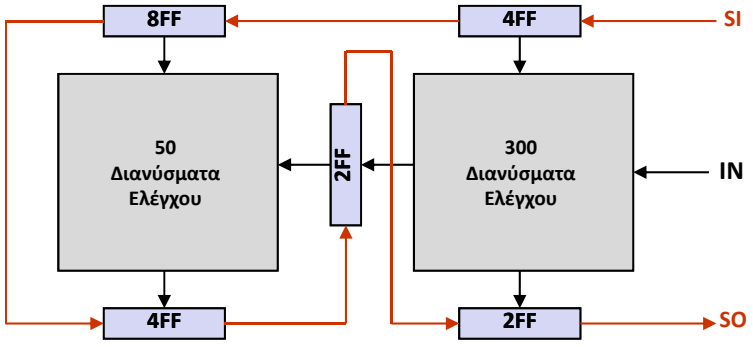
250(12+1)+8 = 3258 clock cycles

4008 clock cycles

Improvement 37% !

Reordering of Scan Chain Flip-Flops (III)

3rd Alternative Scan Testing Application with cell reordering



Test Application: 50(18+1) = 950 clock cycles

250(4+1)+4 = 1254 clock cycles

2204 clock cycles

Improvement 65% !

In addition, test power reduction is achieved!

References

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