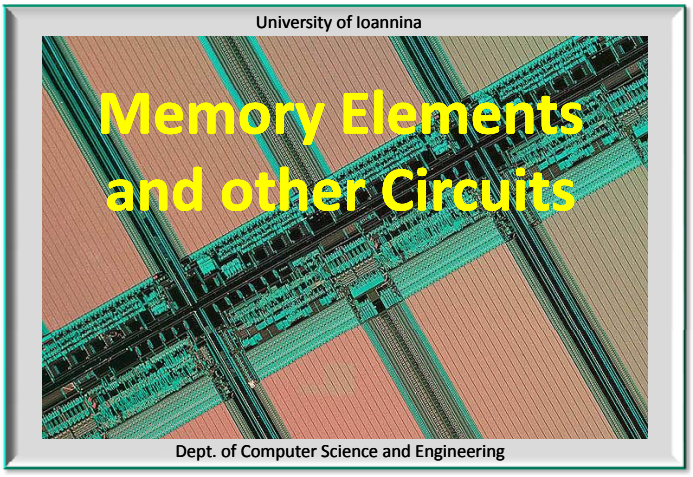
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES



Y. Tsiatouhas

CMOS Integrated Circuit Design Techniques

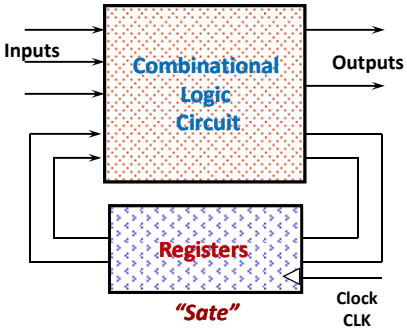
Overview

1. ***Bi-stable circuits – Metastability***
2. ***Latches – Flip-Flops***
3. ***Pipelines***
4. ***Mono-stable circuits***
5. ***Clock generators – The PLL***
6. ***Schmitt trigger circuits***
7. ***Charge pumps***

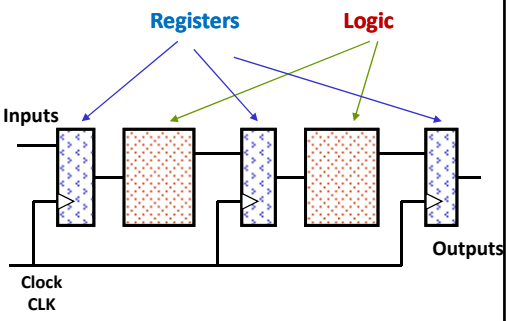
VLSI Systems
and Computer Architecture Lab

Sequential Logic

outputs= f(inputs, state)

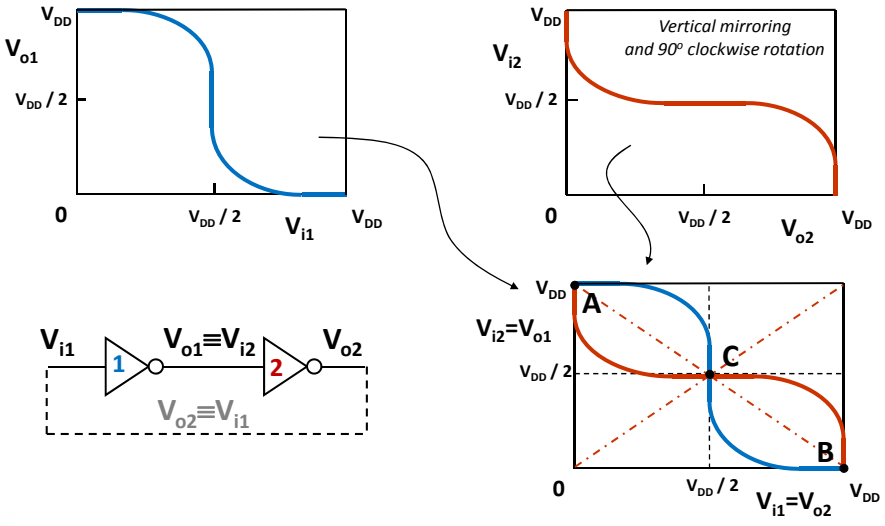


Finite State Machine – FSM

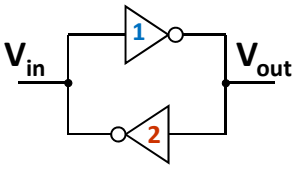


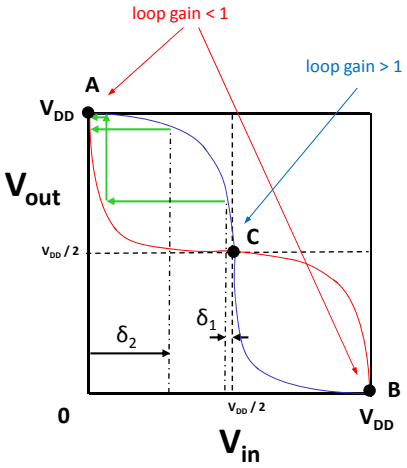
Pipeline

Bistable Circuits' Operating Principle



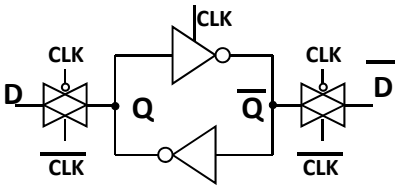
Metastable & Stable Operating Points

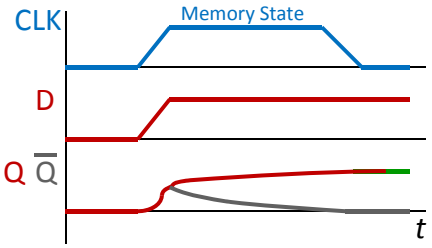




A and B = stable operating points
C = metastable operating point

Metastability



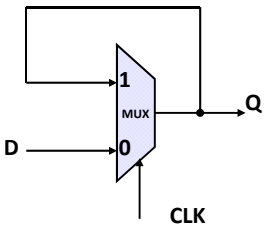


In case that signals D and $\overline{D}$ are making transitions almost concurrently with the clock signal CLK, then the following scenario is possible: the clock signal enters the memory state while the voltage level of both internal nodes $\overline{Q}$ and Q is close to the transition threshold of the two inverters. As a result the latch will arrive to its final state after a quite long time interval, while the logic level of this state depends on random factors, like the noise!

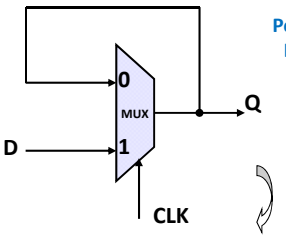
Latches

Multiplexer Based Latch

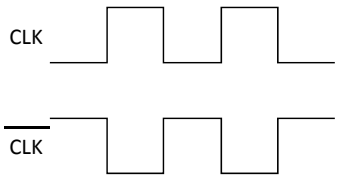
Negative Latch



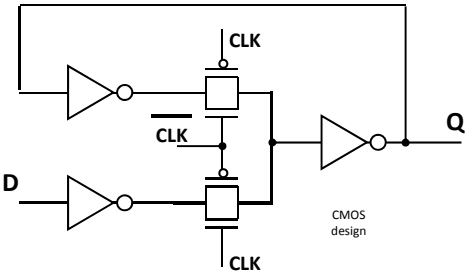
Positive Latch



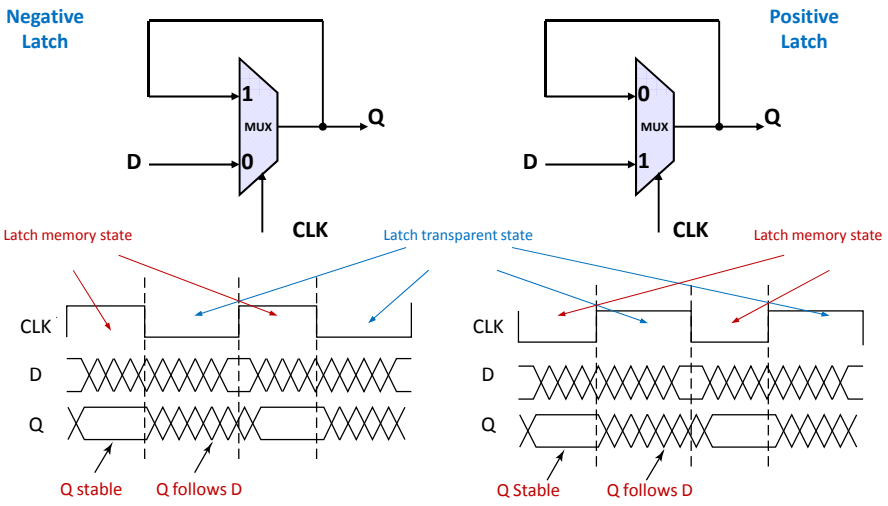
Latch: Level-sensitive circuit



Complementary (non overlapping) clock

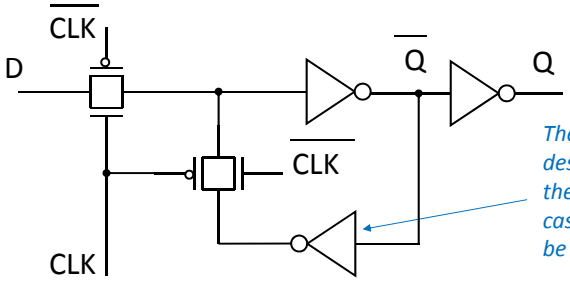


Latch Timing



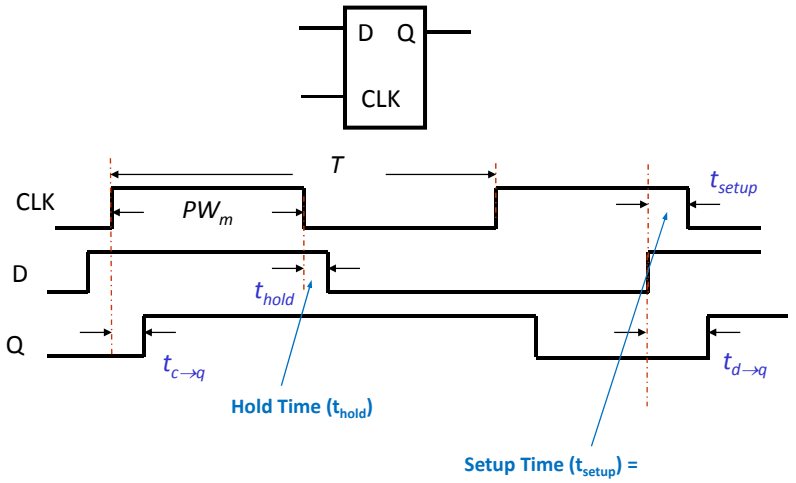
Controllable Feedback Latch

A D-latch is sensitive to the level of the clock signal CLK. One level stands for the *transparent mode of operation* where the input data pass to the circuit output Q. The other level stands for the *memory mode of operation* where the latch output Q holds the last value of the D input before the transition of the clock from the transparency level to the memory level.

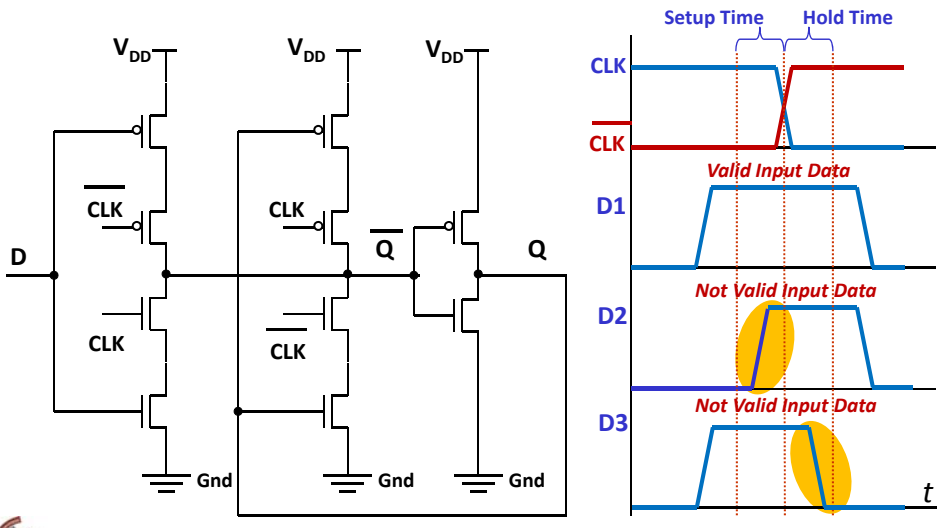


The feedback inverter can be designed with the $k_{p,n}$ factor of the transistors to be small. In that case the following pass-gate can be eliminated.

Latch Timing Characteristics

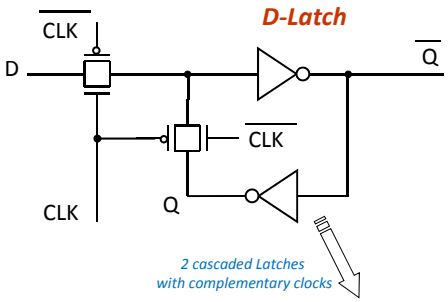


Feedback D Latch

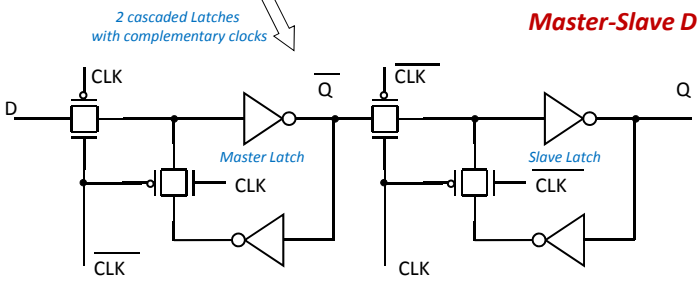


Flip Flops

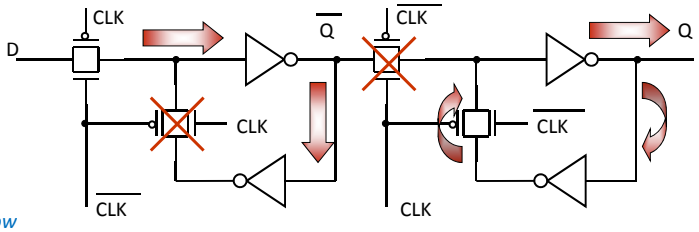
Master-Slave D Flip–Flop



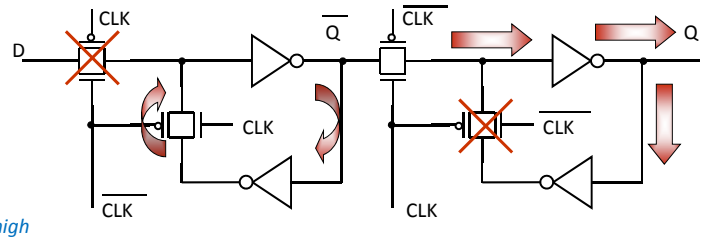
A Flip-Flop is an *edge-triggered* memory element. It is sensitive to a clock edge and not to a clock level. Only at this specific edge the input data pass to the output.



Master-Slave D Flip-Flop Operation

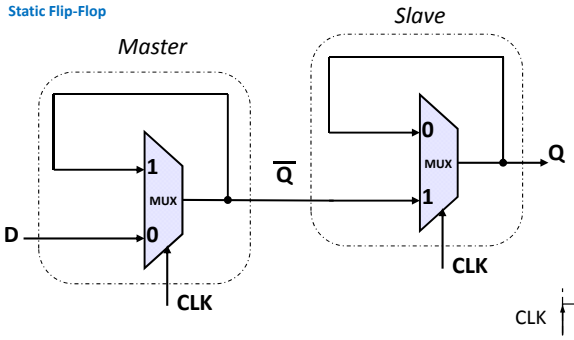


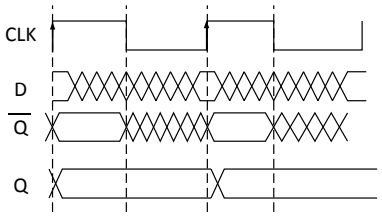
CLK = "0" - low



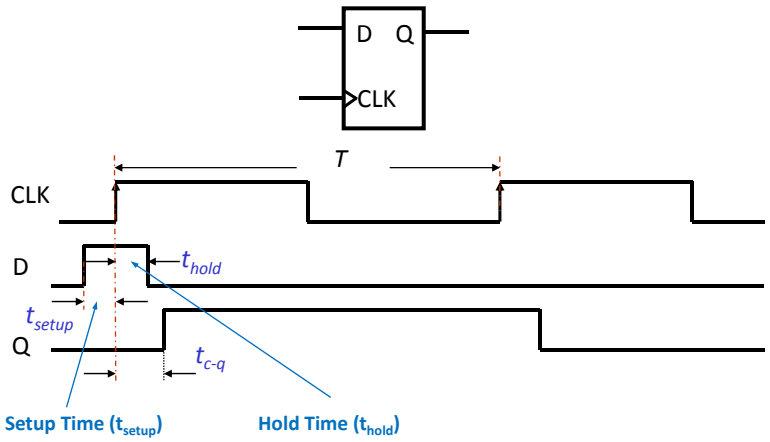
CLK = "1" - high

Multiplexer Based D Flip-Flop

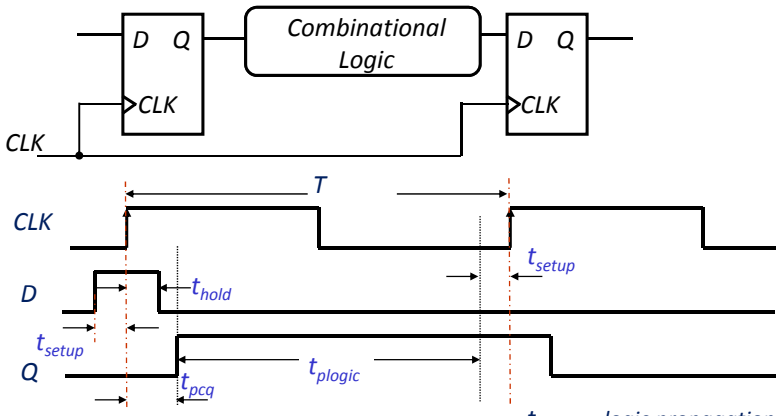




D Flip-Flop Timing Characteristics



D Flip-Flop Timing



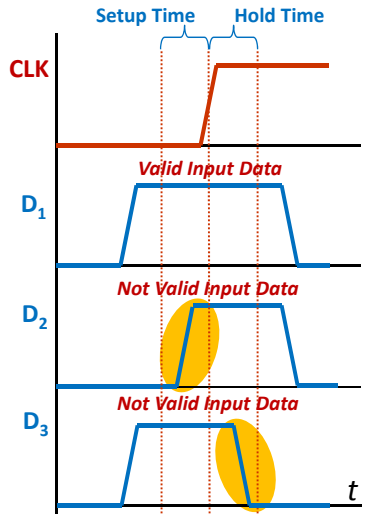
t_{plogic} = logic propagation delay (worst case)

Must stand that: $T \geq t_{pcq} + t_{plogic} + t_{setup}$

and $t_{hold} \leq t_{cdflip\text{-}flop} + t_{cdlogic}$

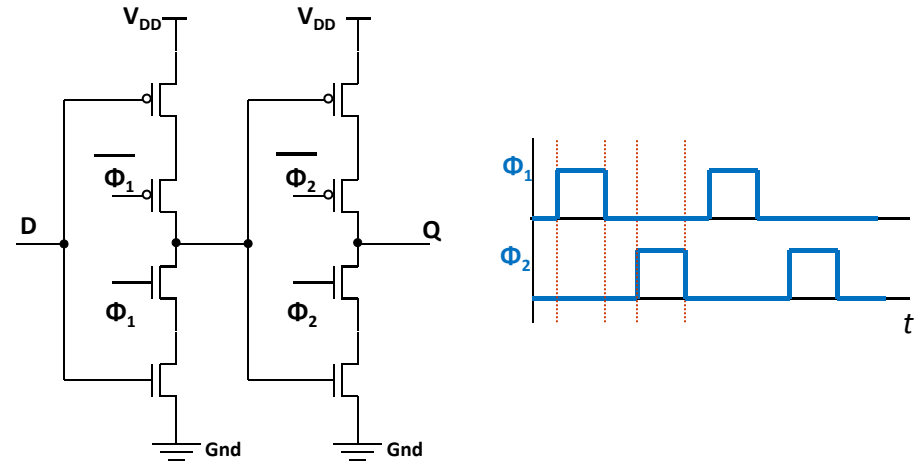
$t_{cdflip\text{-}flop}$ / $t_{cdlogic}$ = minimum delay (contamination delay) flip-flop/logic

Setup and Hold Times

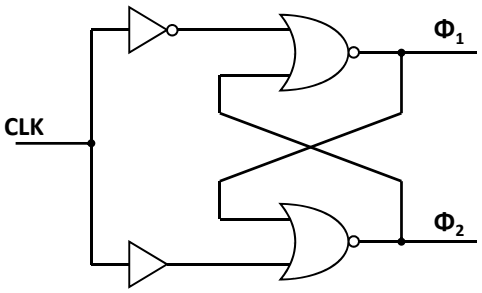


Two-Phase C²MOS D Flip-Flop

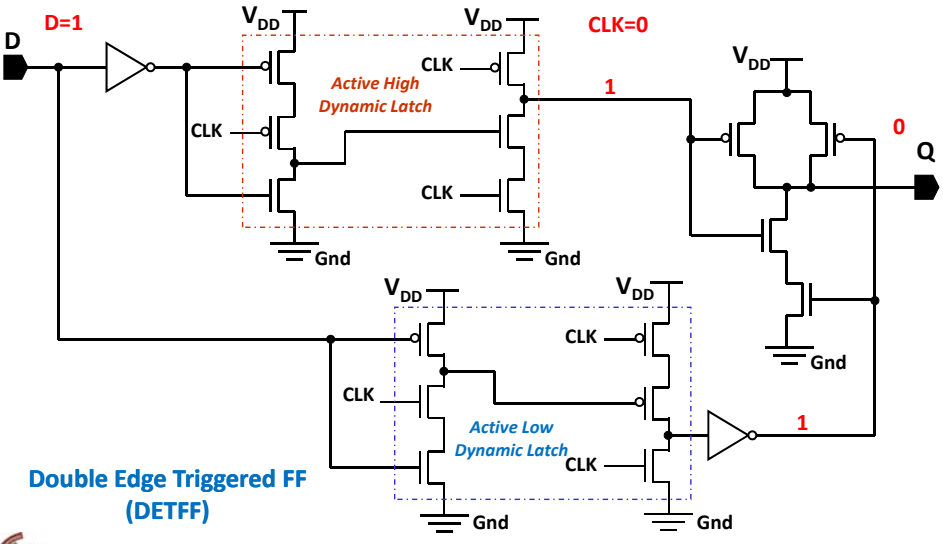
Dynamic Flip-Flop



Non-Overlapping Phases Generation

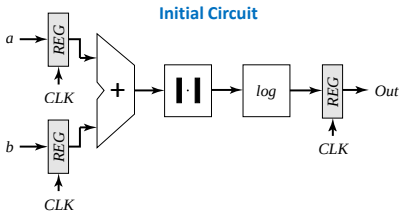


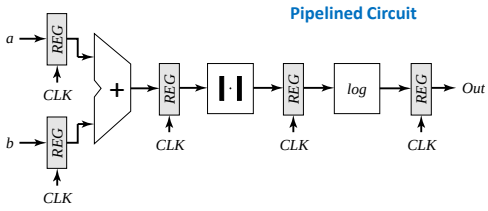
Double Edge Triggered Flip-Flop



Double Edge Triggered FF
(DETFF)

Pipelines I





$$T_{min,org} = t_{c\to q} + \left(t_{p\_add} + t_{p\_abs} + t_{p\_log}\right) + t_{su}$$

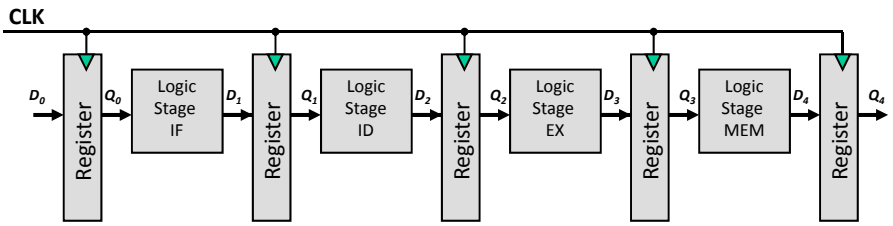
$$T_{min,pipe} = t_{c\to q} + \max\left(t_{p\_add}, t_{p\_abs}, t_{p\_log}\right) + t_{su}$$

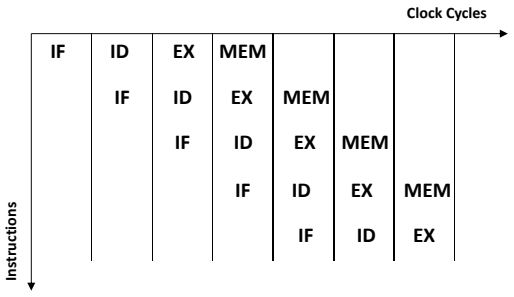
in case that $t_{p\_add} = t_{p\_abs} = t_{p\_log}$

then $T_{min,pipe} \cong T_{min,org}/3$

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\lvert a_1 + b_1 \rvert$	
3	$a_3 + b_3$	$\lvert a_2 + b_2 \rvert$	$\log(\lvert a_1 + b_1 \rvert)$
4	$a_4 + b_4$	$\lvert a_3 + b_3 \rvert$	$\log(\lvert a_2 + b_2 \rvert)$
5	$a_5 + b_5$	$\lvert a_4 + b_4 \rvert$	$\log(\lvert a_3 + b_3 \rvert)$

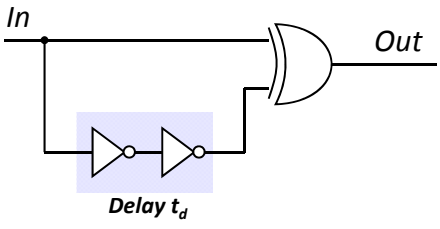
Pipelines II

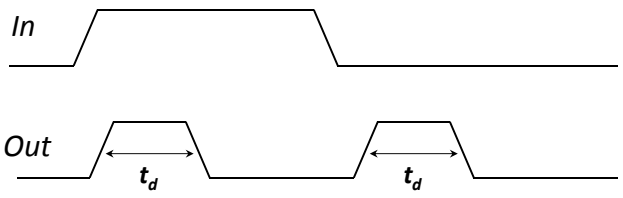




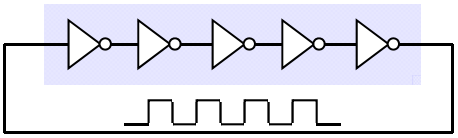
Other Circuits

Monostable Circuits





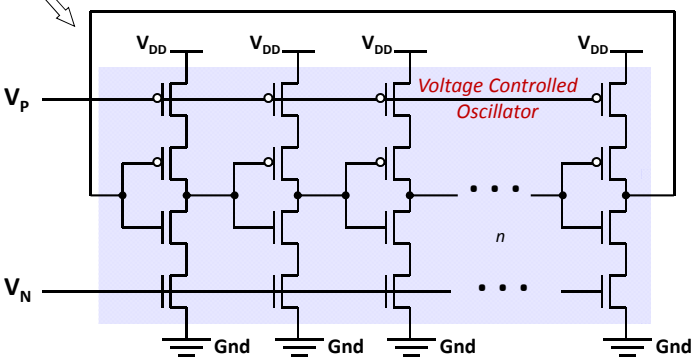
Non-Stable Circuits



Ring Oscillator

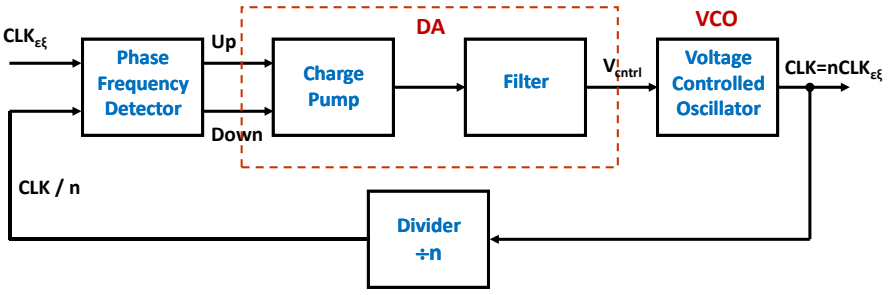
$$f_{osc} = \frac{1}{n \cdot (t_{d0\to1} + t_{d1\to0})}$$

n = # βαθμίδων



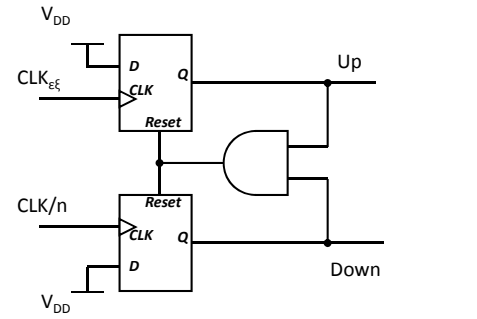
Clock Generation

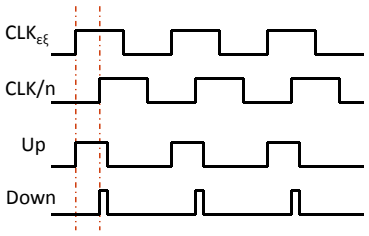
Phase Locked Loops (PLLs)

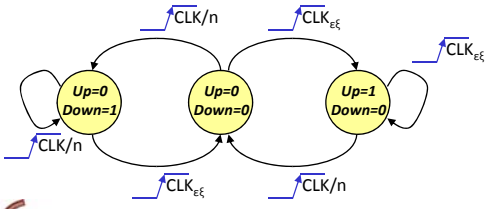


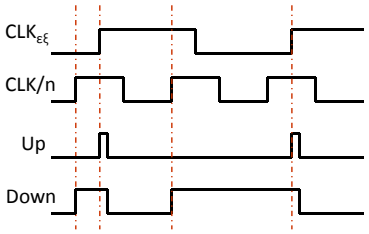
- High frequency clock CLK generation from a low frequency reference clock $CLK_{\epsilon\xi}$

Phase – Frequency Detector I

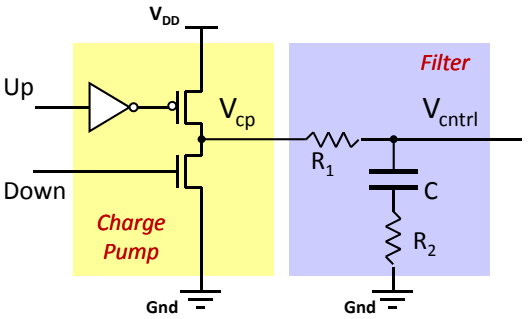


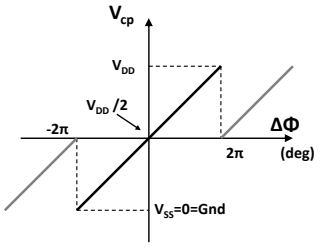






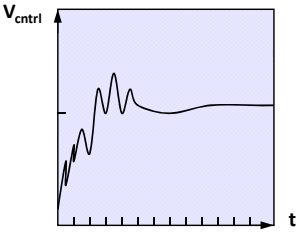
Charge Pump and Filter II





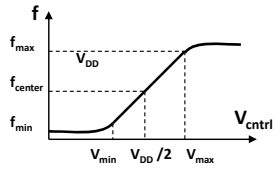
$$V_{cp} = \frac{V_{DD} - 0}{4\pi}\Delta\Phi$$

Filter Transfer Function: $$V_{cntrl} = \frac{1 + j\omega R_2 C}{1 + j\omega(R_1 + R_2)C} V_{cp}$$

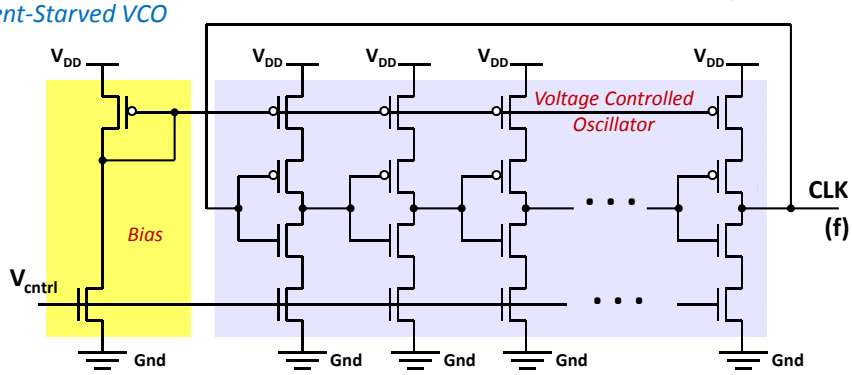


Voltage Controlled Oscillator (VCO) III

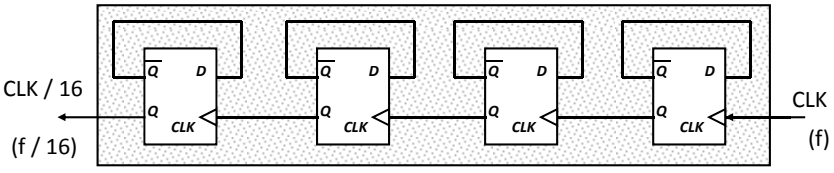
Curve slope: $K_{VCO} = 2\pi \frac{f_{max} - f_{min}}{V_{max} - V_{min}}$



Current-Starved VCO



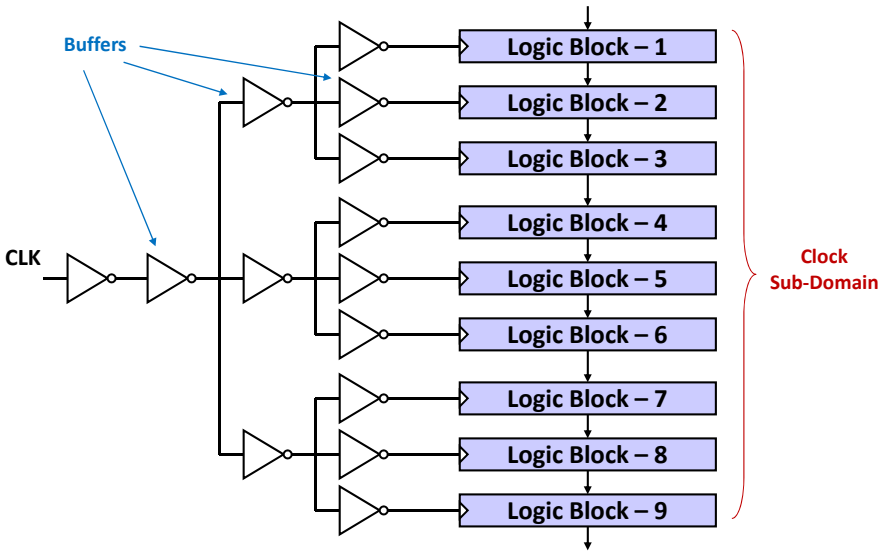
Frequency Divider IV



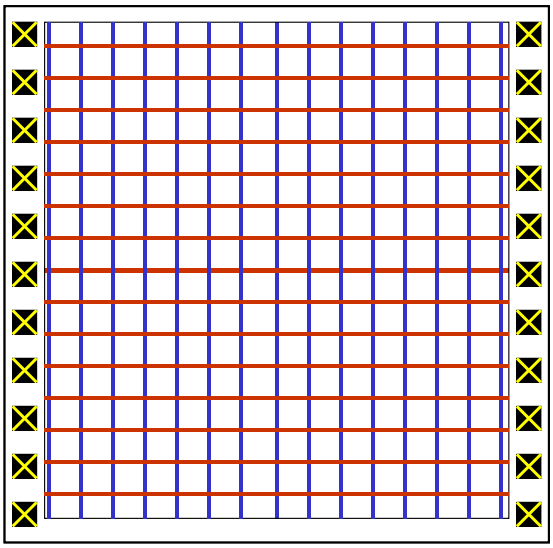
Binary Counter

$$f = \frac{1}{T_{CLK}}$$

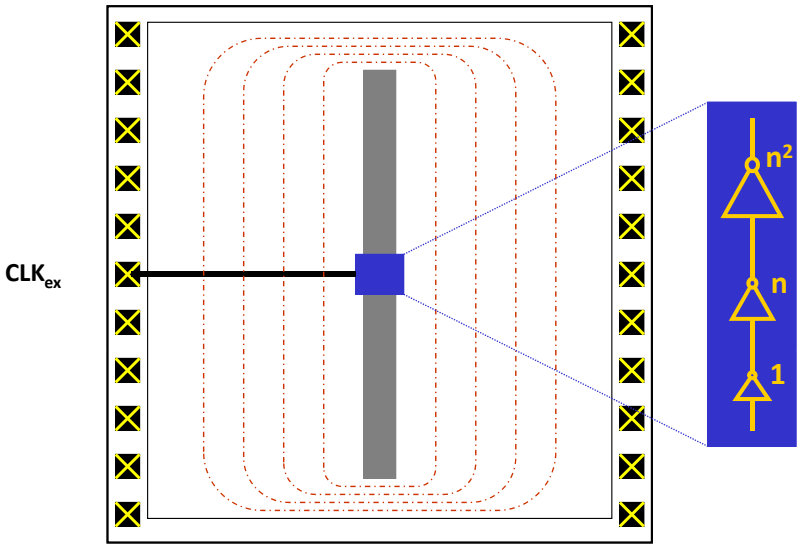
Clock Distribution



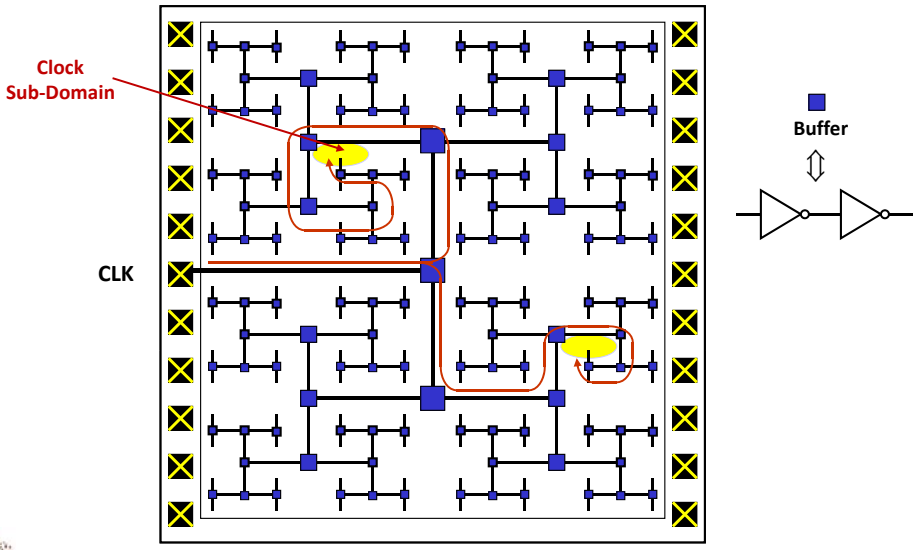
Grid Clock Distribution



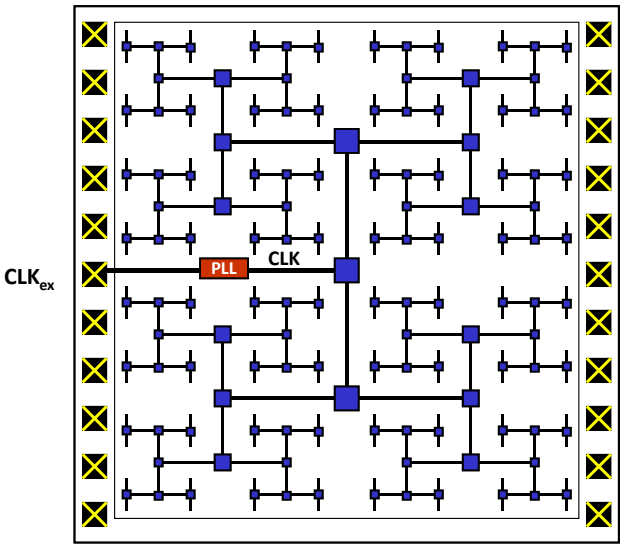
Central Clock Distribution



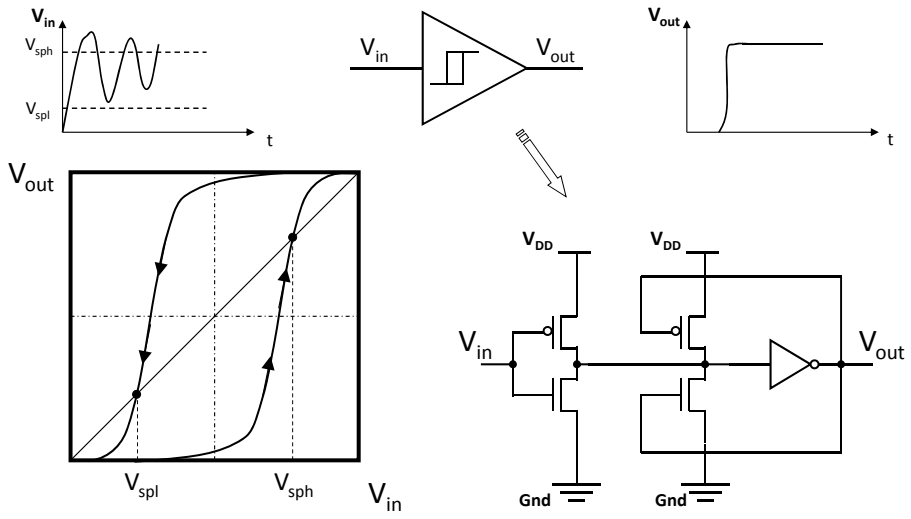
H-Tree Clock Distribution (I)



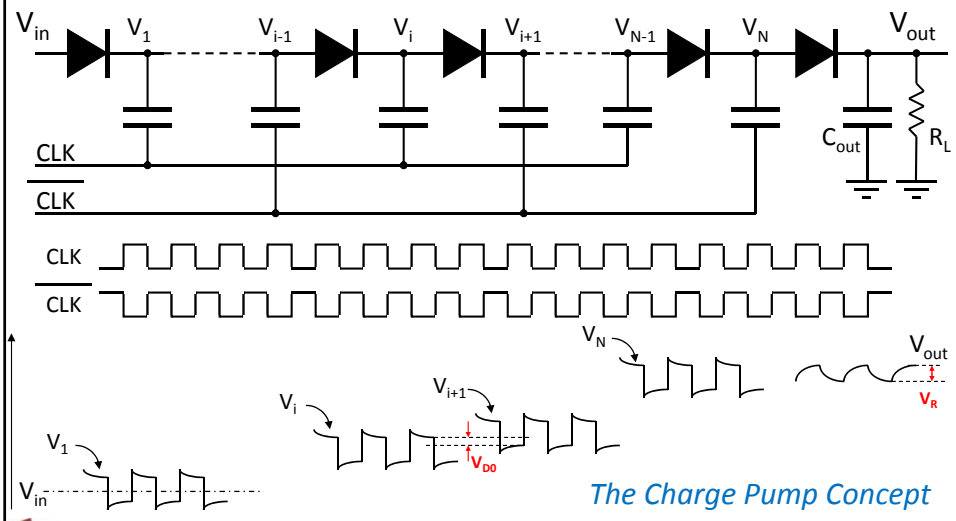
H-Tree Clock Distribution (II)



The Schmitt Trigger Circuit

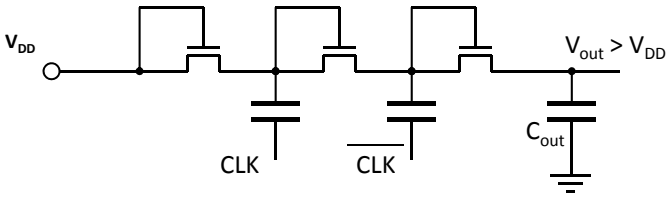


Voltage Generators

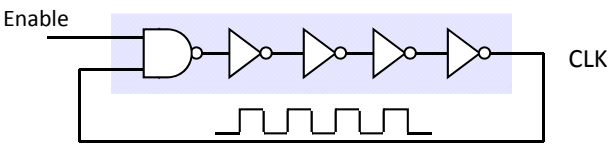


The Charge Pump Concept

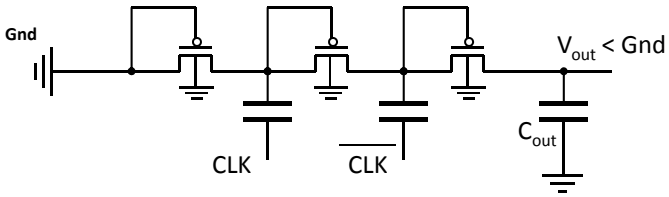
MOS Positive Charge Pump

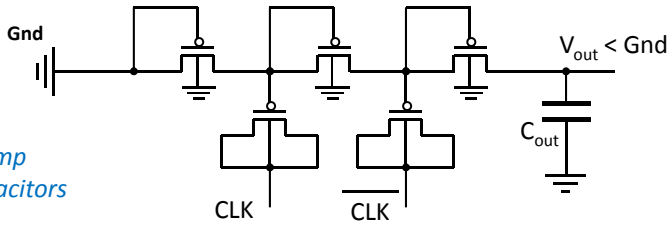


Ring Oscillator with Enable



MOS Negative Charge Pump





Charge Pump with MOS Capacitors