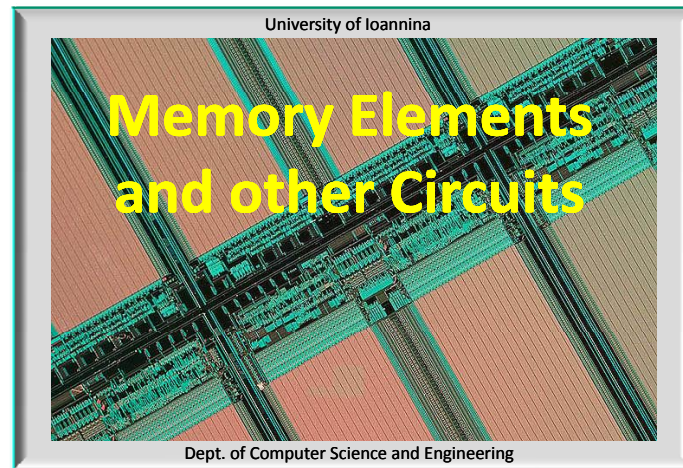


CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES



Y. Triantouhas



CMOS Integrated Circuit Design Techniques

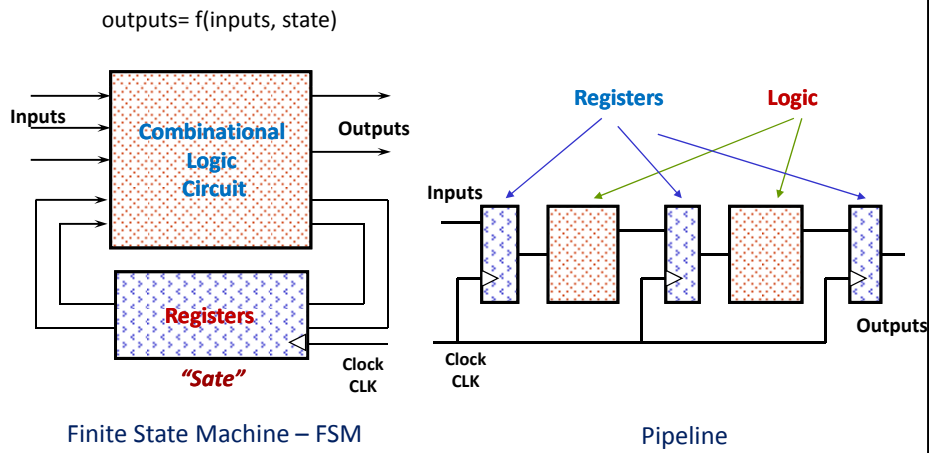
Overview



VLSI Systems
and Computer Architecture Lab

1. *Bi-stable circuits – Metastability*
2. *Latches – Flip-Flops*
3. *Pipelines*
4. *Mono-stable circuits*
5. *Clock generators – The PLL*
6. *Schmitt trigger circuits*
7. *Charge pumps*

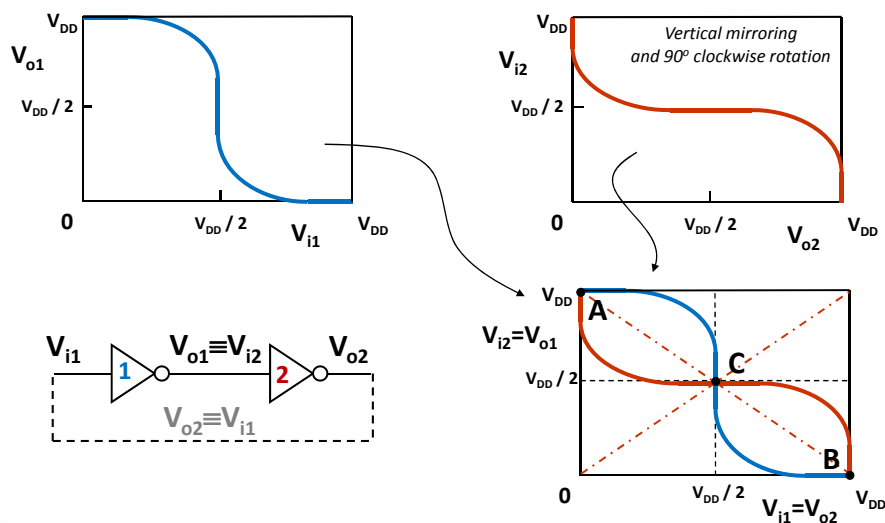
Sequential Logic



Memory Elements

3

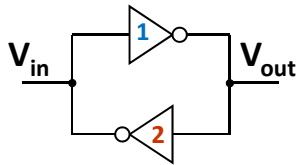
Bistable Circuits' Operating Principle



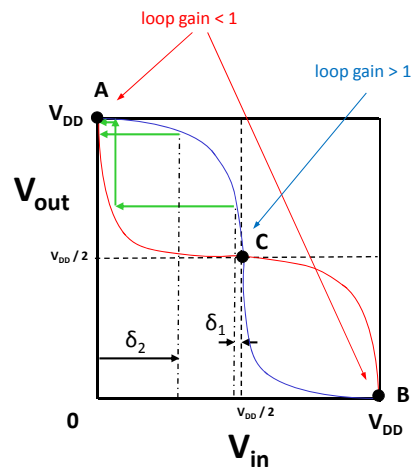
Memory Elements

4

Metastable & Stable Operating Points



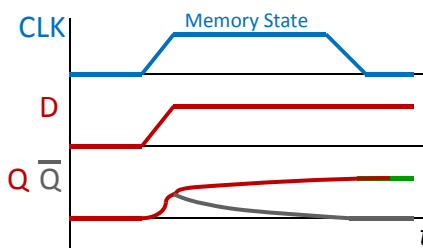
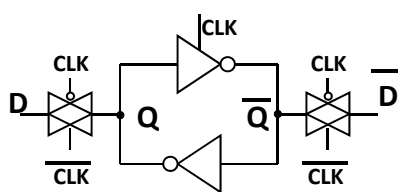
A and B = stable operating points
C = metastable operating point



Memory Elements

5

Metastability



In case that signals D and $\overline{D}$ are making transitions almost concurrently with the clock signal CLK , then the following scenario is possible: the clock signal enters the memory state while the voltage level of both internal nodes $\overline{Q}$ and Q is close to the transition threshold of the two inverters. As a result the latch will arrive to its final state after a quite long time interval, while the logic level of this state depends on random factors, like the noise!



Memory Elements

6

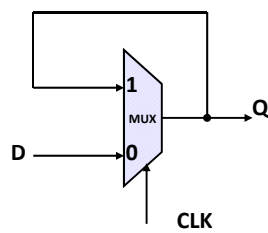
Latches

Memory Elements

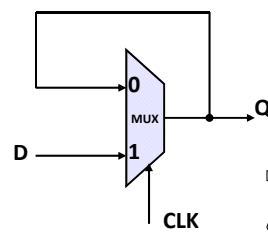
7

Multiplexer Based Latch

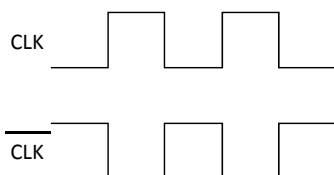
Negative Latch



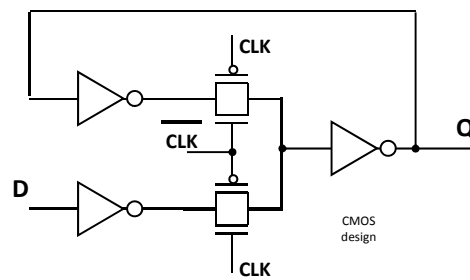
Positive Latch



Latch: Level-sensitive circuit



Complementary (non overlapping) clock

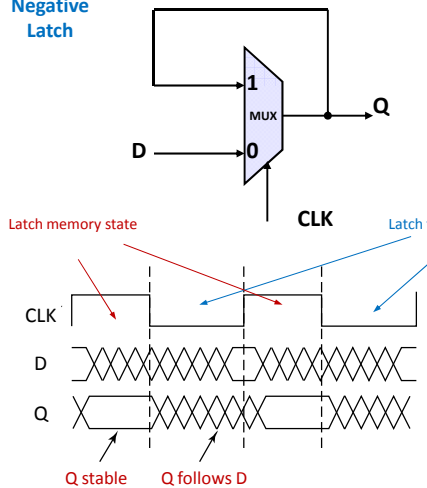


Memory Elements

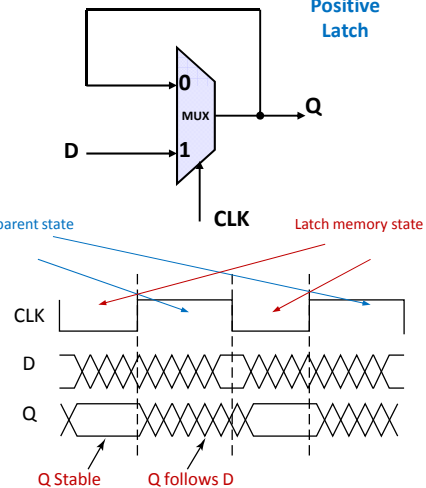
8

Latch Timing

Negative Latch



Positive Latch

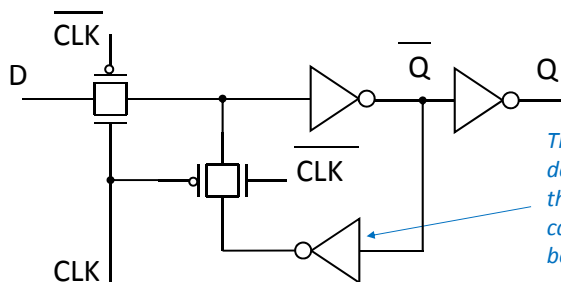


Memory Elements

9

Controllable Feedback Latch

A D-latch is sensitive to the level of the clock signal CLK. One level stands for the *transparent mode of operation* where the input data pass to the circuit output Q. The other level stands for the *memory mode of operation* where the latch output Q holds the last value of the D input before the transition of the clock from the transparency level to the memory level.

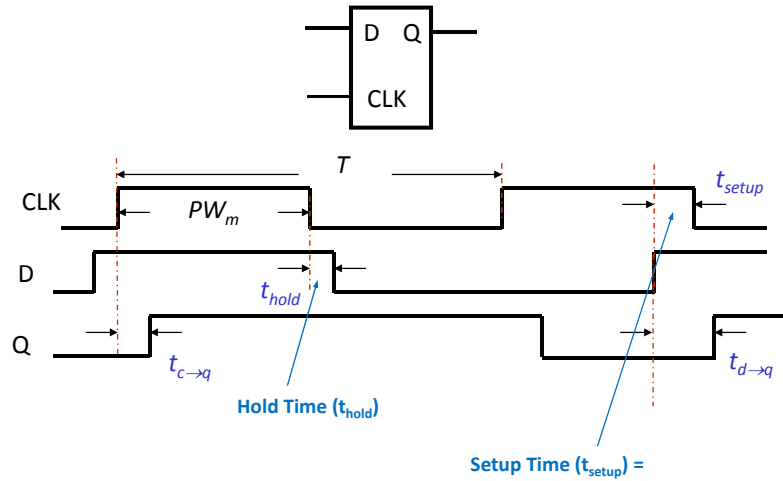


The feedback inverter can be designed with the $k_{p,n}$ factor of the transistors to be small. In that case the following pass-gate can be eliminated.

Memory Elements

10

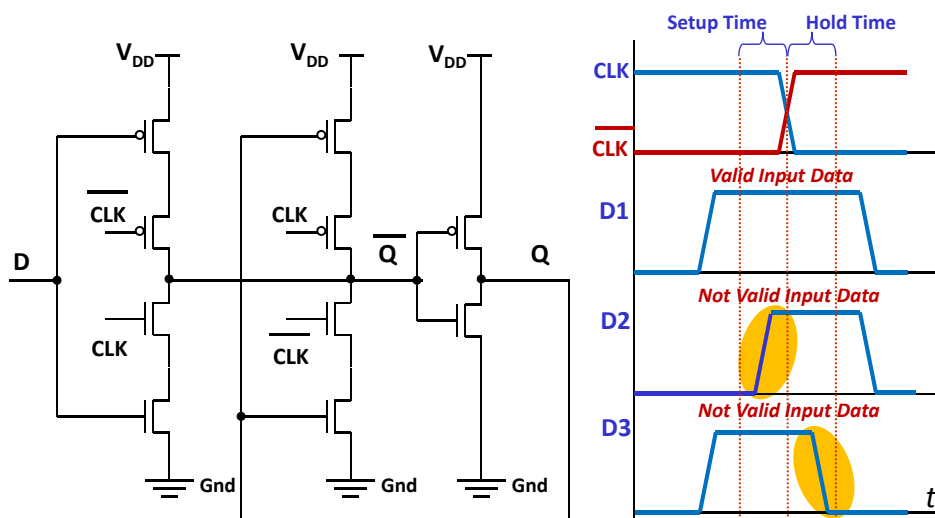
Latch Timing Characteristics



Memory Elements

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Feedback D Latch



Memory Elements

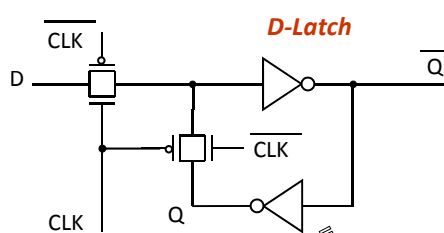
12

Flip Flops

Memory Elements

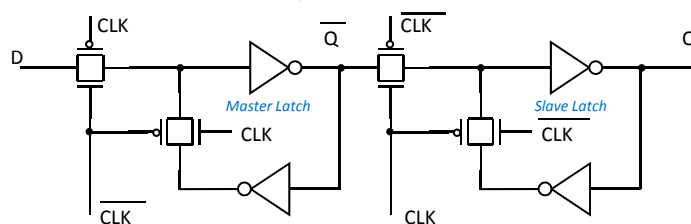
13

Master-Slave D Flip-Flop



A Flip-Flop is an *edge-triggered* memory element. It is sensitive to a clock edge and not to a clock level. Only at this specific edge the input data pass to the output.

2 cascaded Latches
with complementary clocks

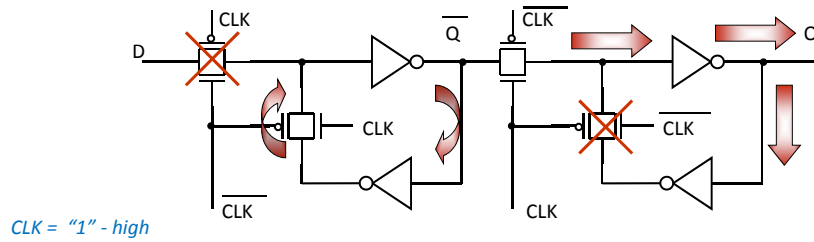
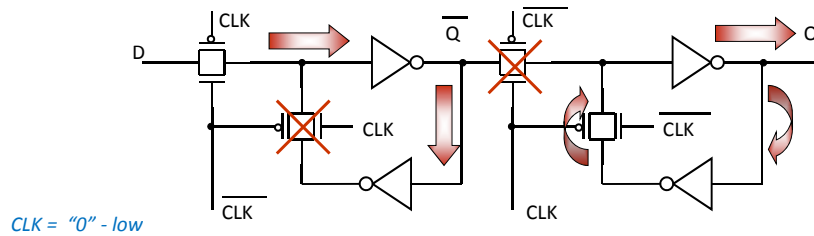


Static Flip-Flop

Memory Elements

14

Master-Slave D Flip-Flop Operation

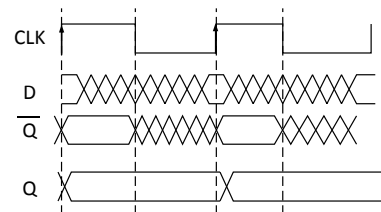
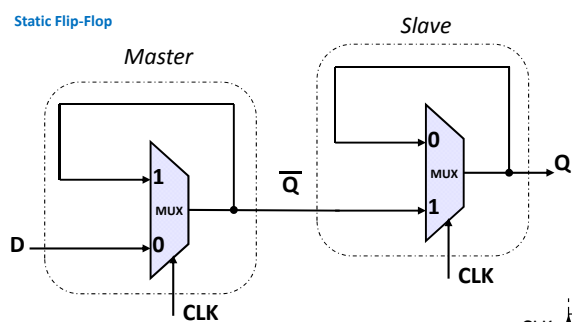


Memory Elements

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Multiplexer Based D Flip-Flop

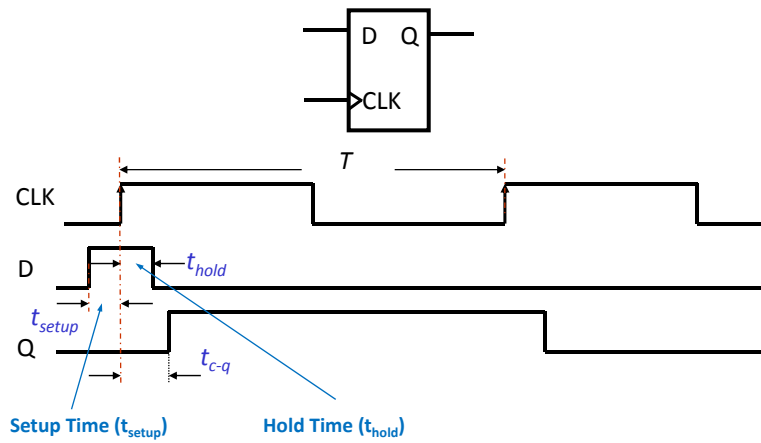
Static Flip-Flop



Memory Elements

16

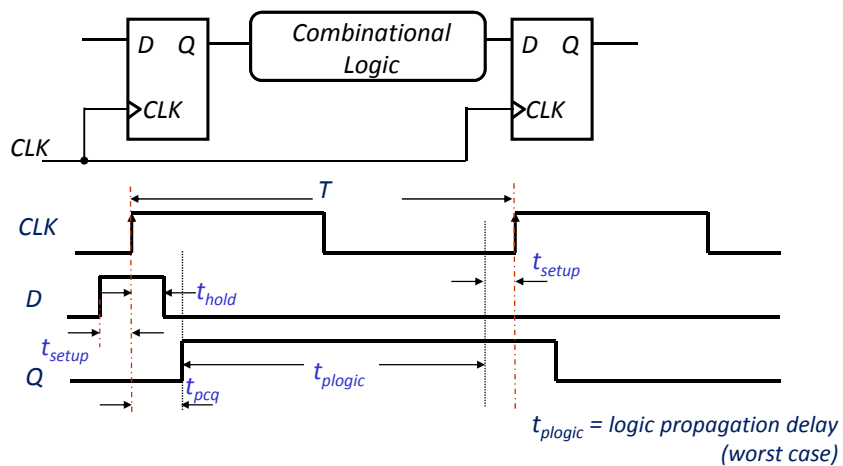
D Flip-Flop Timing Characteristics



Memory Elements

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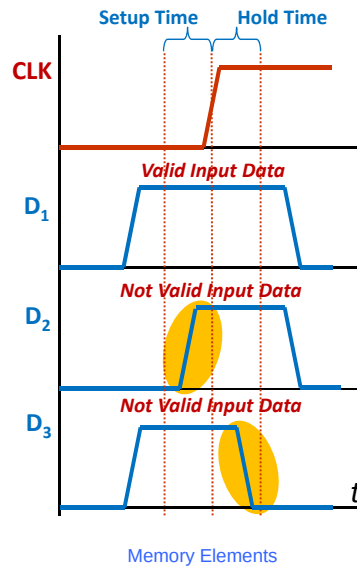
D Flip-Flop Timing



Memory Elements

18

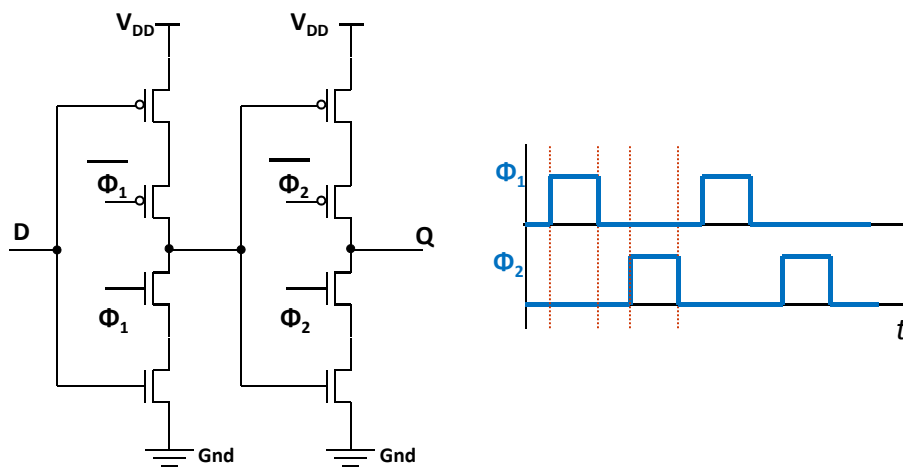
Setup and Hold Times



19

Two-Phase C²MOS D Flip-Flop

Dynamic Flip-Flop



Memory Elements

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Non-Overlapping Phases Generation

The diagram illustrates a circuit for generating two non-overlapping clock phases, Φ_1 and Φ_2 , from a single input clock signal labeled CLK. The CLK signal is split into two parallel paths. The upper path consists of an inverter followed by an OR gate. The lower path consists of an inverter followed by an OR gate. The outputs of these two OR gates are Φ_1 and Φ_2 respectively. The circuit is designed such that Φ_1 and Φ_2 are non-overlapping, meaning they are never both high at the same time.

Memory Elements

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21

Double Edge Triggered Flip-Flop

The diagram illustrates a Double Edge Triggered Flip-Flop (DETFF) circuit. It consists of two dynamic latches and a cross-coupled output stage.

- Input D:** The data input signal, shown as a square wave.
- Active High Dynamic Latch:** A dashed red box highlights the top latch. It has two clock inputs (CLK) and one data input (D). The output of this latch is labeled **1**.
- Active Low Dynamic Latch:** A dashed blue box highlights the bottom latch. It has two clock inputs (CLK) and one data input (D). The output of this latch is labeled **1**.
- Output Stage:** The outputs of the two latches are connected to a cross-coupled output stage. The output of the top latch is connected to the input of the bottom latch, and the output of the bottom latch is connected to the input of the top latch. The output of the top latch is labeled **0** and the output of the bottom latch is labeled **1**.
- Power and Ground:** The circuit is powered by V_{DD} and grounded (Gnd).

Double Edge Triggered FF (DETFF)

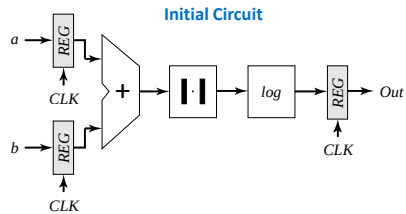
Memory Elements

22



22

Pipelines I

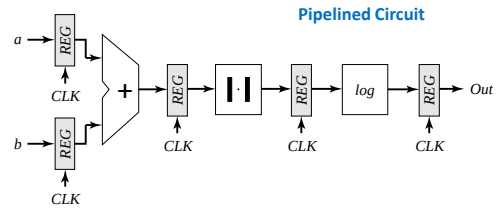


$$T_{\min, \text{org}} = t_{c \rightarrow q} + (t_{p_{\text{add}}} + t_{p_{\text{abs}}} + t_{p_{\text{log}}}) + t_{\text{su}}$$

$$T_{\min, \text{pipe}} = t_{c \rightarrow q} + \max(t_{p_{\text{add}}}, t_{p_{\text{abs}}}, t_{p_{\text{log}}}) + t_{\text{su}}$$

in case that $t_{p_{\text{add}}} = t_{p_{\text{abs}}} = t_{p_{\text{log}}}$

$$\text{then } T_{\min, \text{pipe}} \cong \frac{T_{\min, \text{org}}}{3}$$



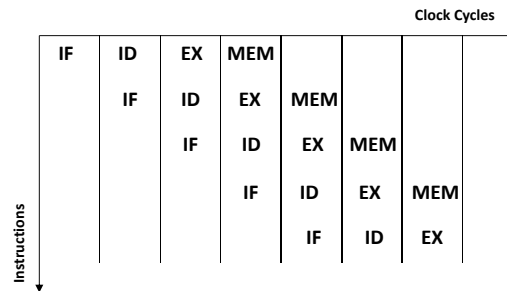
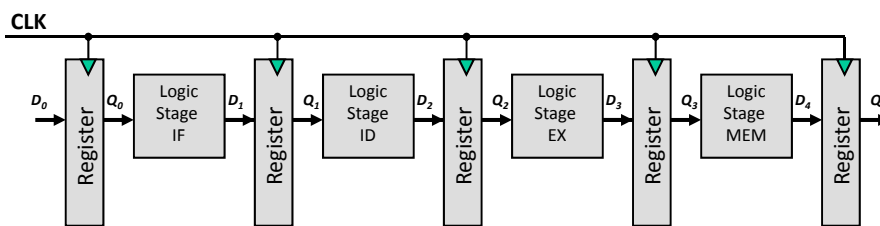
Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$ a_1 + b_1 $	
3	$a_3 + b_3$	$ a_2 + b_2 $	$\log(a_1 + b_1)$
4	$a_4 + b_4$	$ a_3 + b_3 $	$\log(a_2 + b_2)$
5	$a_5 + b_5$	$ a_4 + b_4 $	$\log(a_3 + b_3)$



Memory Elements

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Pipelines II



Memory Elements

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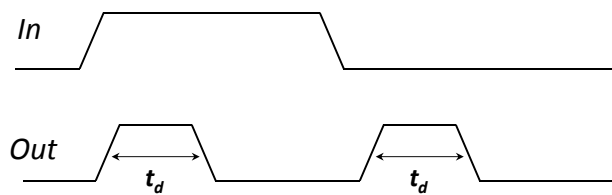
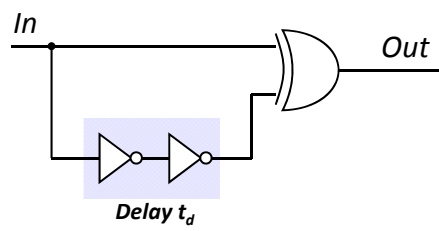
Other Circuits



Memory Elements

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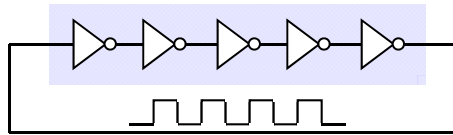
Monostable Circuits



Memory Elements

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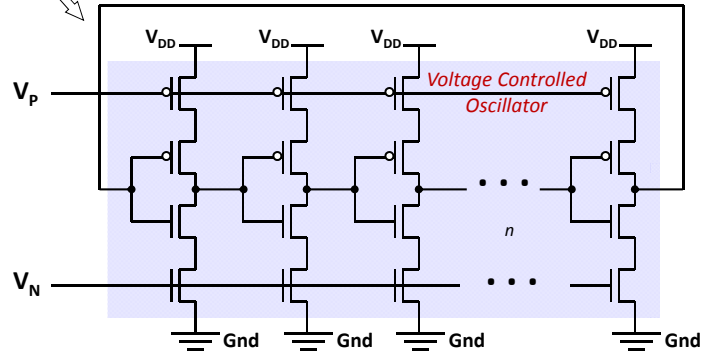
Non-Stable Circuits



Ring Oscillator

$$f_{osc} = \frac{1}{n \cdot (t_{d0 \rightarrow 1} + t_{d1 \rightarrow 0})}$$

$n = \# \text{ \beta \alpha \mu \iota \delta \omega \nu }$

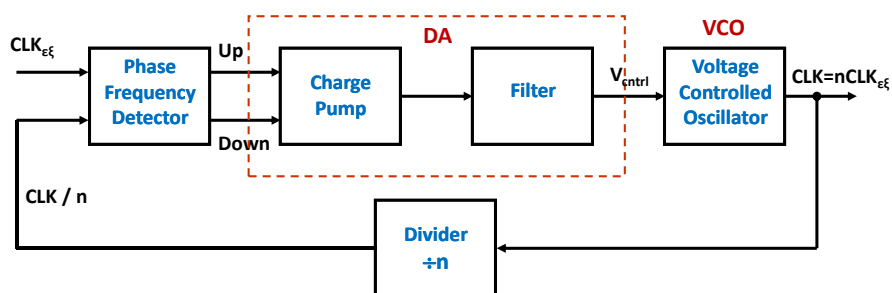


Memory Elements

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Clock Generation

Phase Locked Loops (PLLs)

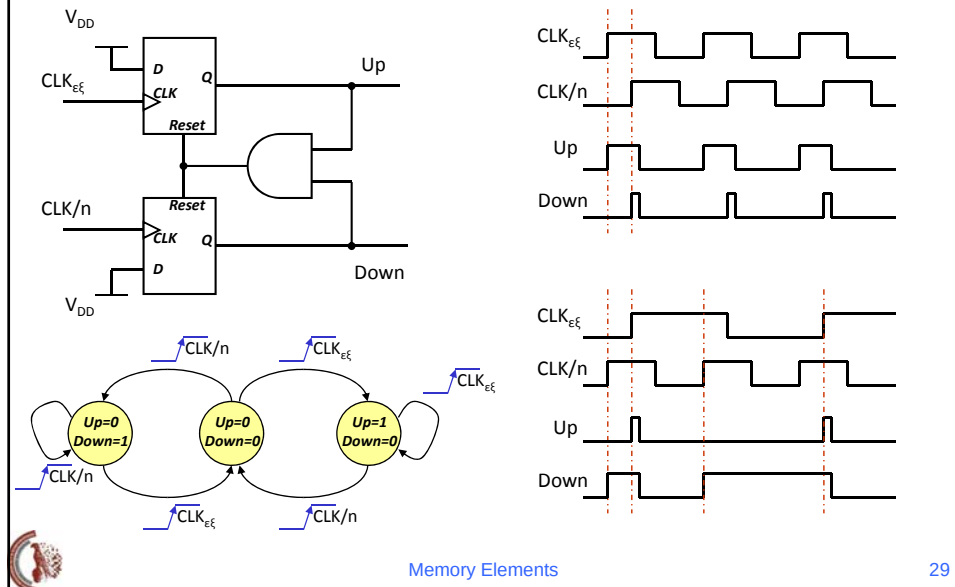


- High frequency clock CLK generation from a low frequency reference clock $CLK_{\epsilon\xi}$

Memory Elements

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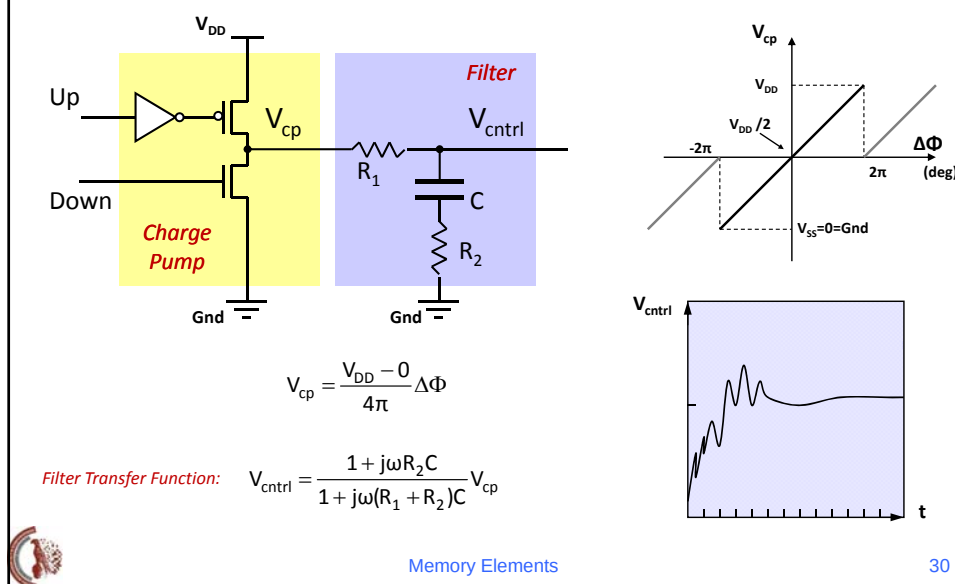
Phase – Frequency Detector I



Memory Elements

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Charge Pump and Filter II

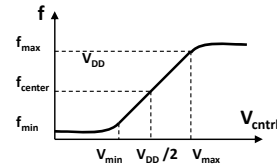


Memory Elements

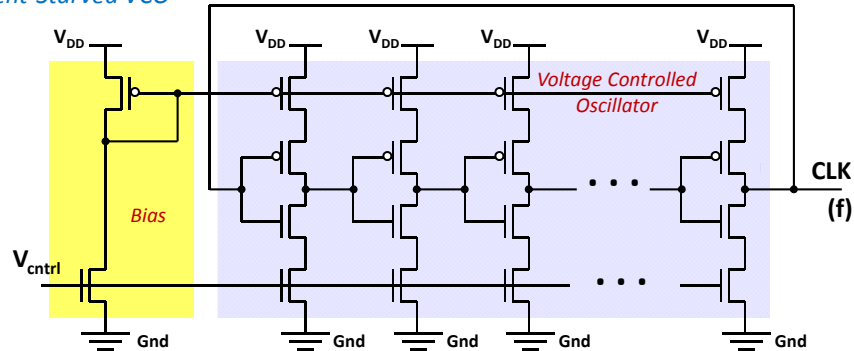
30

Voltage Controlled Oscillator (VCO) III

Curve slope: $K_{VCO} = 2\pi \frac{f_{\max} - f_{\min}}{V_{\max} - V_{\min}}$



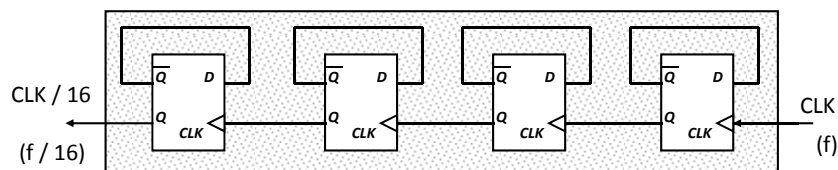
Current-Starved VCO



Memory Elements

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Frequency Divider IV



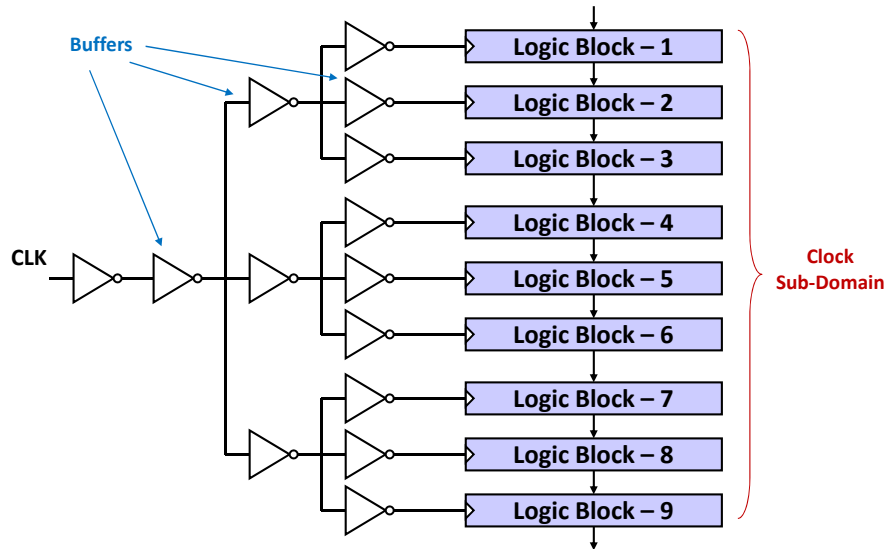
Binary Counter

$$f = \frac{1}{T_{CLK}}$$

Memory Elements

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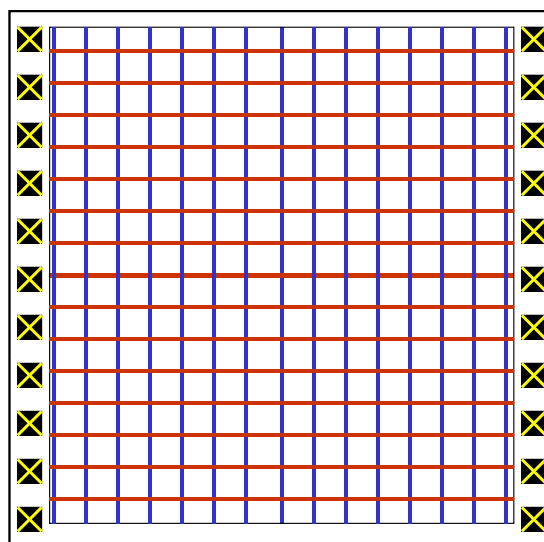
Clock Distribution



Memory Elements

33

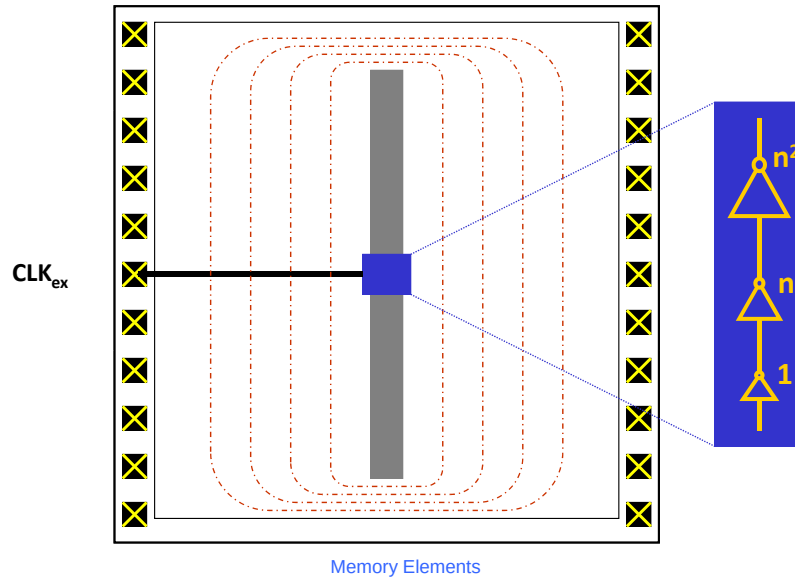
Grid Clock Distribution



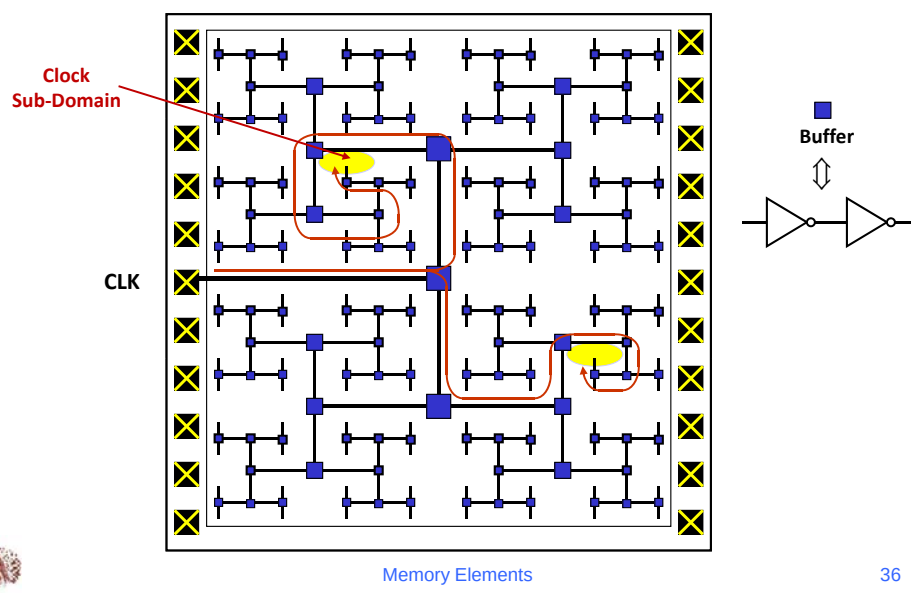
Memory Elements

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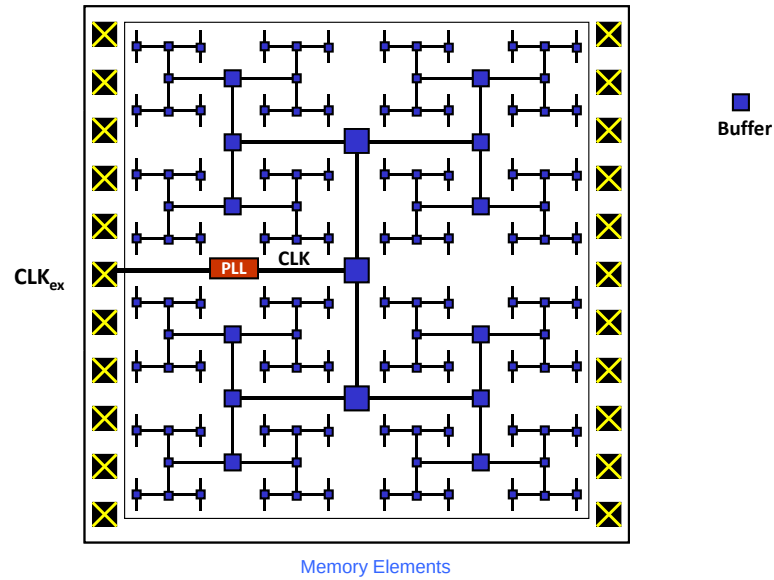
Central Clock Distribution



H-Tree Clock Distribution (I)

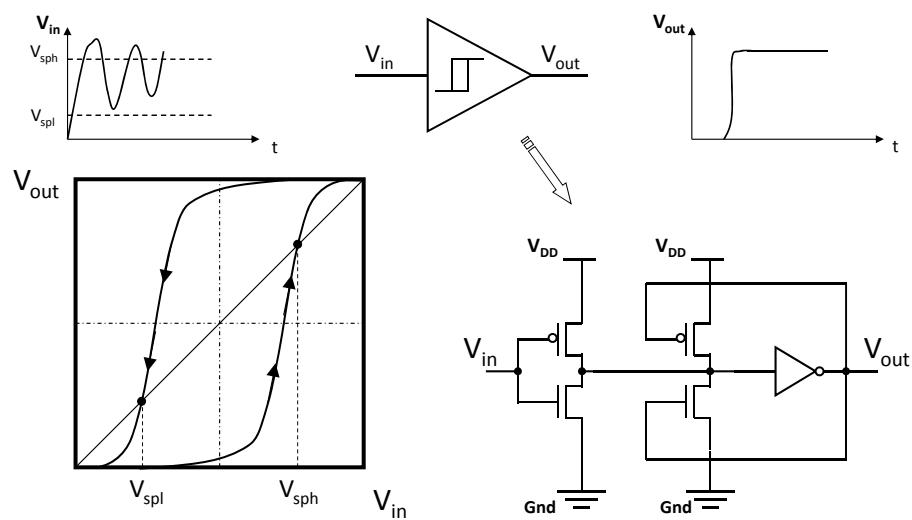


H-Tree Clock Distribution (II)



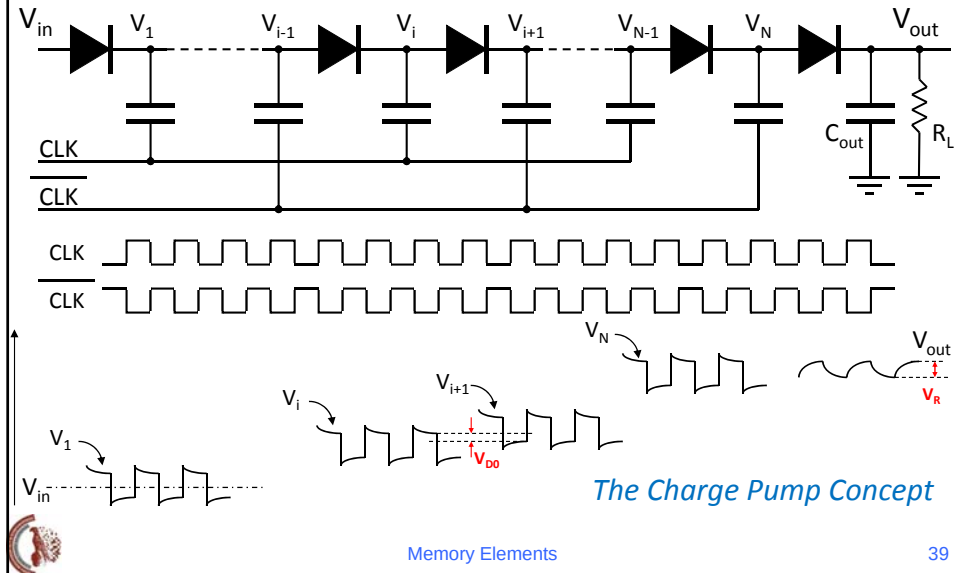
37

The Schmitt Trigger Circuit

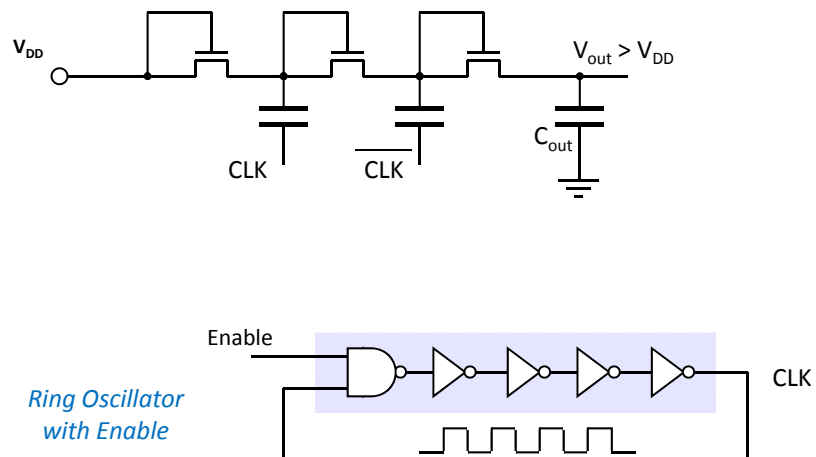


38

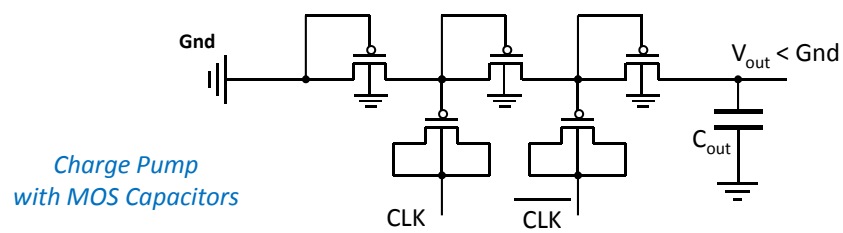
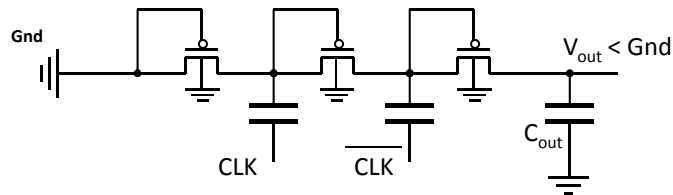
Voltage Generators



MOS Positive Charge Pump



MOS Negative Charge Pump



*Charge Pump
with MOS Capacitors*



Memory Elements

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