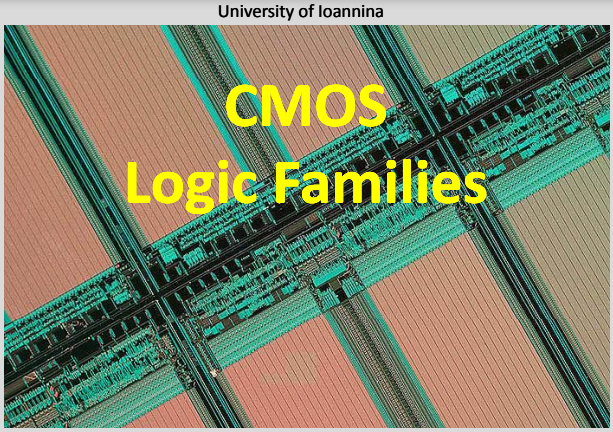
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

University of Ioannina



Dept. of Computer Science and Engineering

Y. Tsiatouhas

CMOS Integrated Circuit Design Techniques

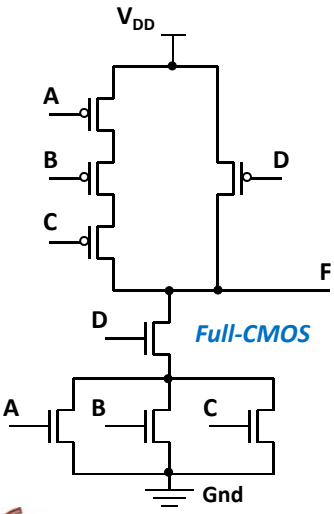
Overview

1. ***Non-clocked CMOS logic families***
2. ***Clocked CMOS logic families***

VLSI Systems
and Computer Architecture Lab

Non-Clocked CMOS Logic Families

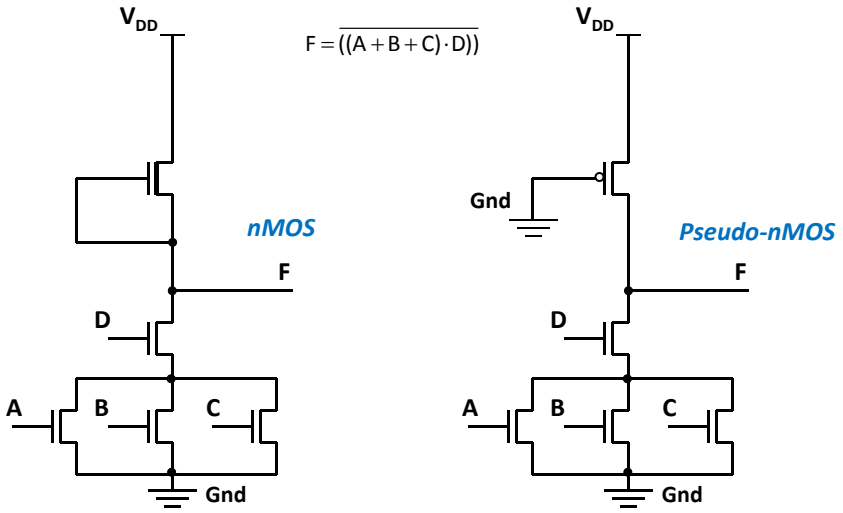
Full or Static CMOS Logic



$$F = \overline{((A + B + C) \cdot D)}$$

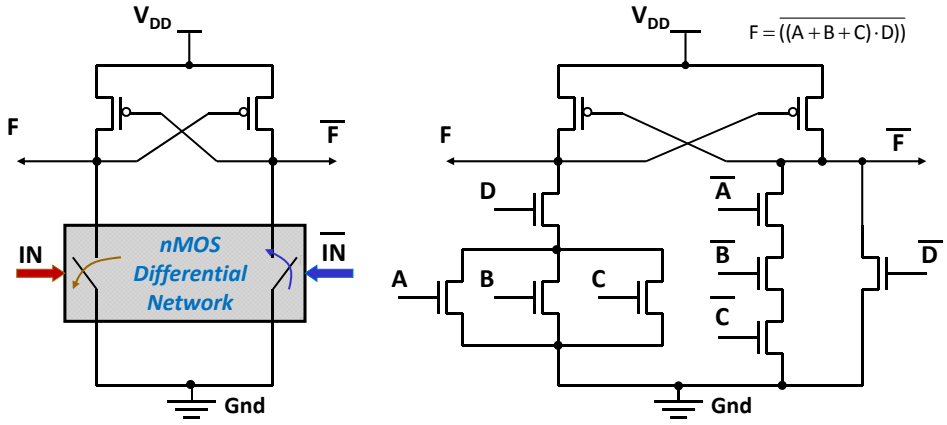
Strengths	Weaknesses
Low Static Power	Overlap Currents
Good Yield/Defect Tolerance	High Fan-Out Loads
High Test Coverage	High Noise Generation
High Noise Immunity	

nMOS and Pseudo-nMOS Logic



Differential Cascode Voltage Switch Logic I

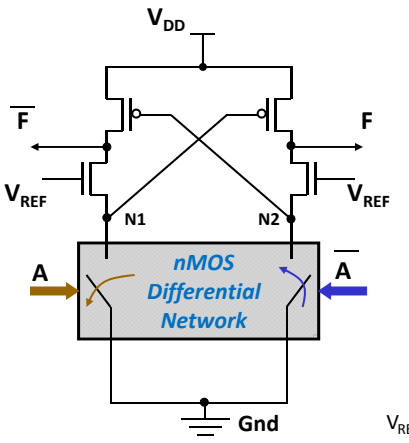
DCVS

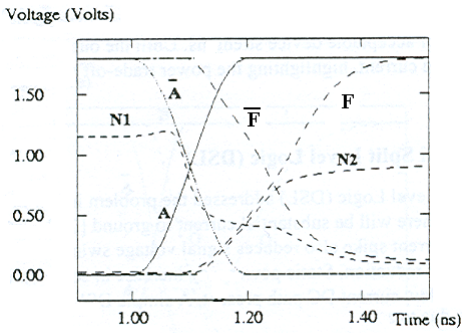


DCVS Logic II

Strengths	Weaknesses
Good Logic Density	Dual Rail Wiring
Complementary Output Availability	pMOS Strength vs Latching Hysterisis
High Reliability	High Device Count (depending on applic.)
High Noise Immunity	

Differential Split-Level (DSL) Logic I



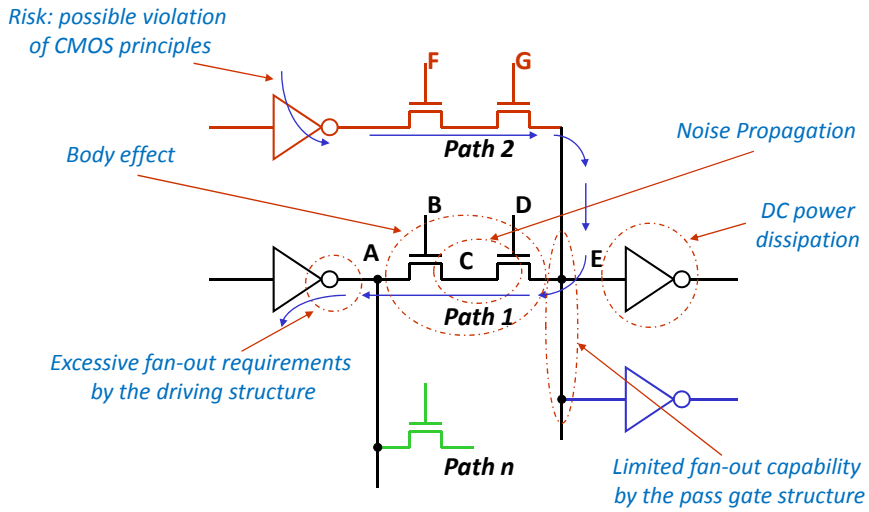


$$V_{REF} = \frac{V_{DD}}{2} + V_{tn}$$

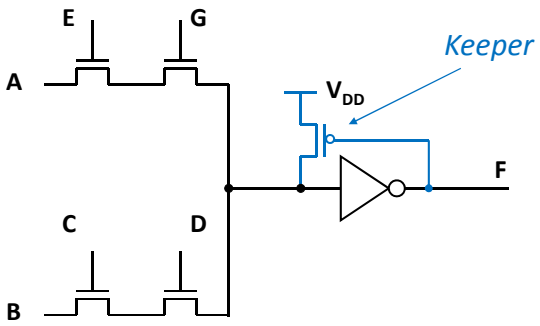
DSL Logic II

Strengths	Weaknesses
Low Switching Power Dissipation	High Static Power Dissipation
Complementary Output Availability	V_{REF} Generation
High Reliability	High Device Count

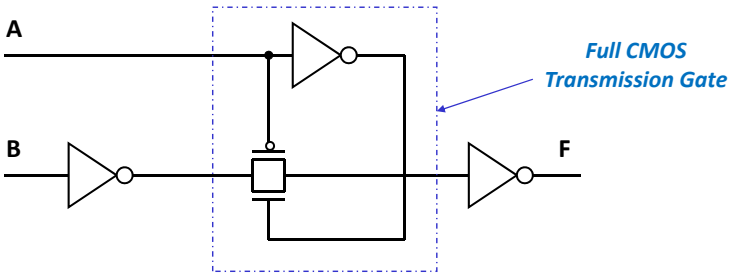
Pass Gate Logic



Keeper Based Pass Gate Logic

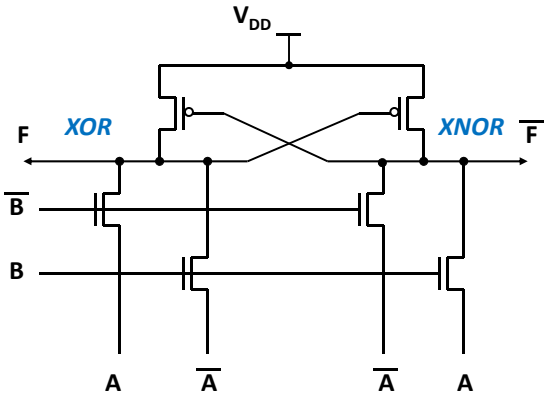


Full CMOS Transmission Gate Logic



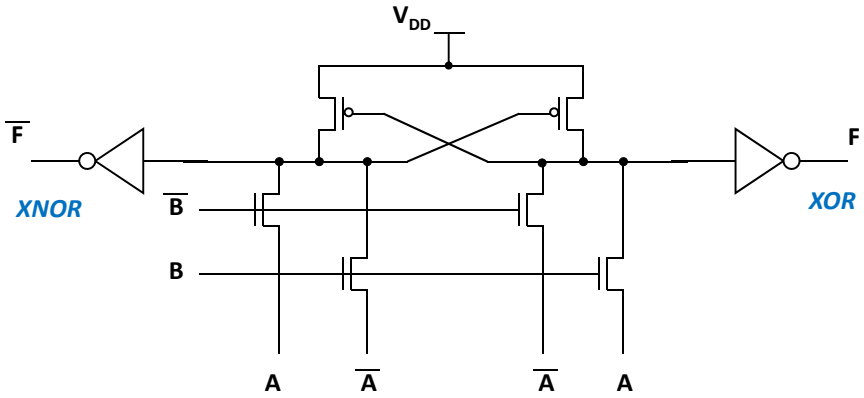
Strengths	Weaknesses
High Speed	Body Effect
Low Area	Limited Logic Depth
Low Power	

DCVS Logic with Pass Gates



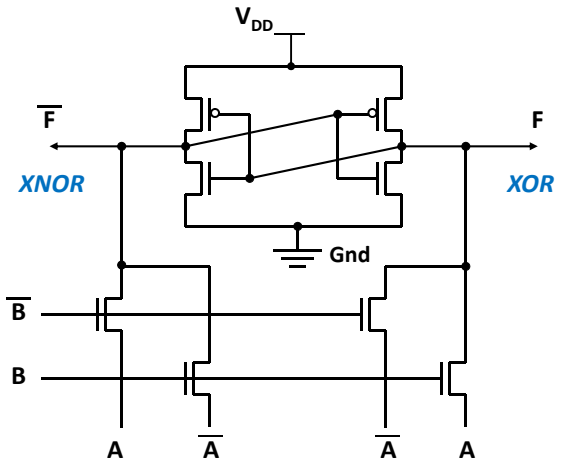
Strengths	Weaknesses
Full Swing	Limited Logic Depth
Noise Immunity	Limited Load Drive
Area-Power Reduction	Body Effect
No Floating Nodes	

Complementary Pass Gate Logic (CPL)



High Speed Operation

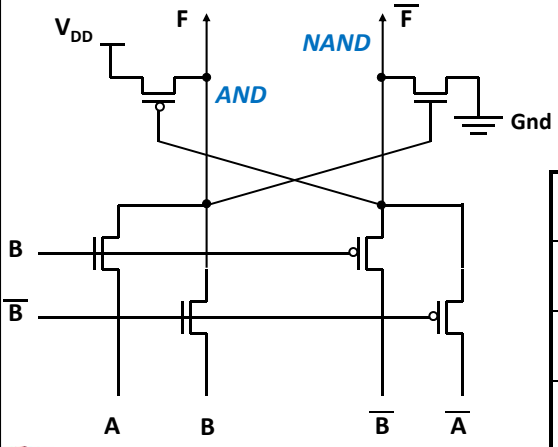
Swing-Restored Pass Gate Logic (SRPL) I

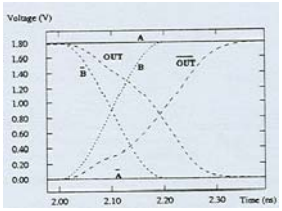


SRPL Logic II

Strengths	Weaknesses
Low Static Power Dissipation	Limited Output Load
Process Tolerance	Overlapping Current
Sense Amplifier Speed Performance	Drive Strength vs Performance
High Logic Depth	

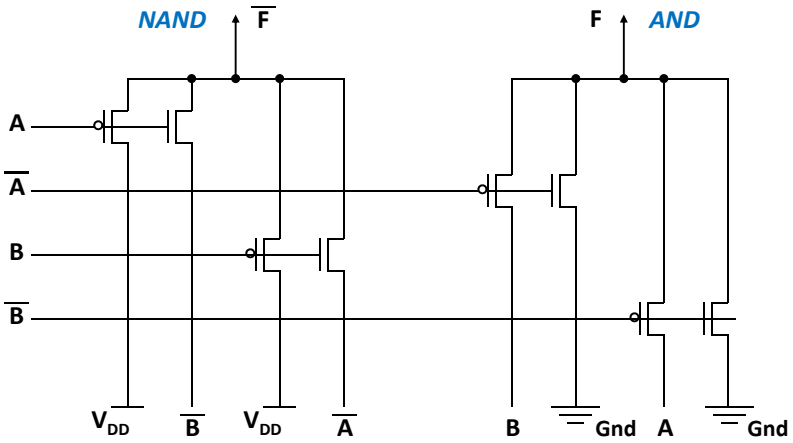
Push-Pull Pass Transistor Logic (PPL)





Strengths	Weaknesses
Low Power	pMOS Logic Implementation
Hysterisis Elimination	Limited Sequential Usage
	Limited Fun-Out Capability

Double Pass Transistor Logic (DPL) I

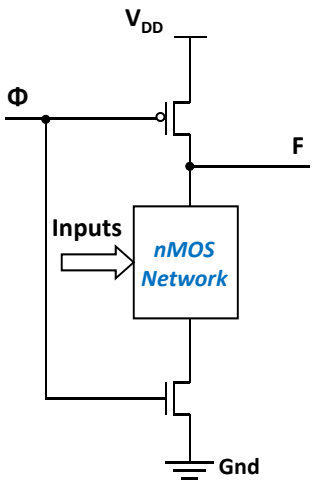


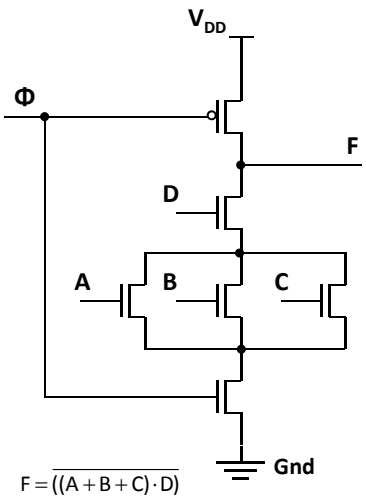
DPL Logic II

Strengths	Weaknesses
High Speed Operation	Limited Logic Depth
No V_{th} Drops	Limited Load Capability
	Redundant Device Structure

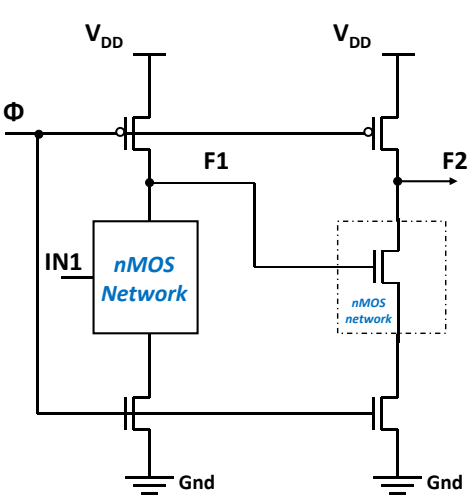
Clocked CMOS Logic Families

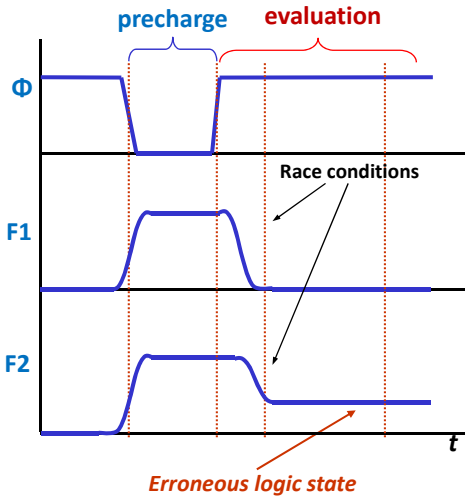
Dynamic CMOS Logic I



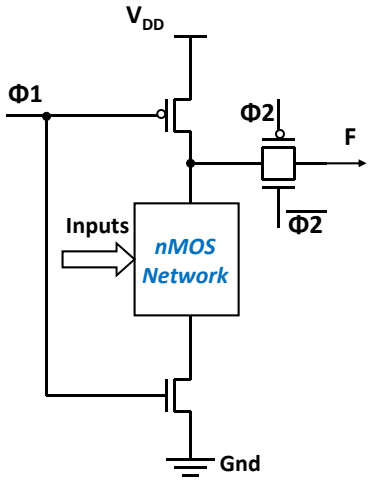


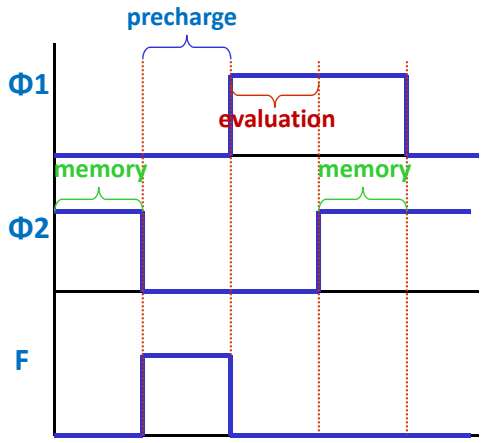
Dynamic CMOS Logic II



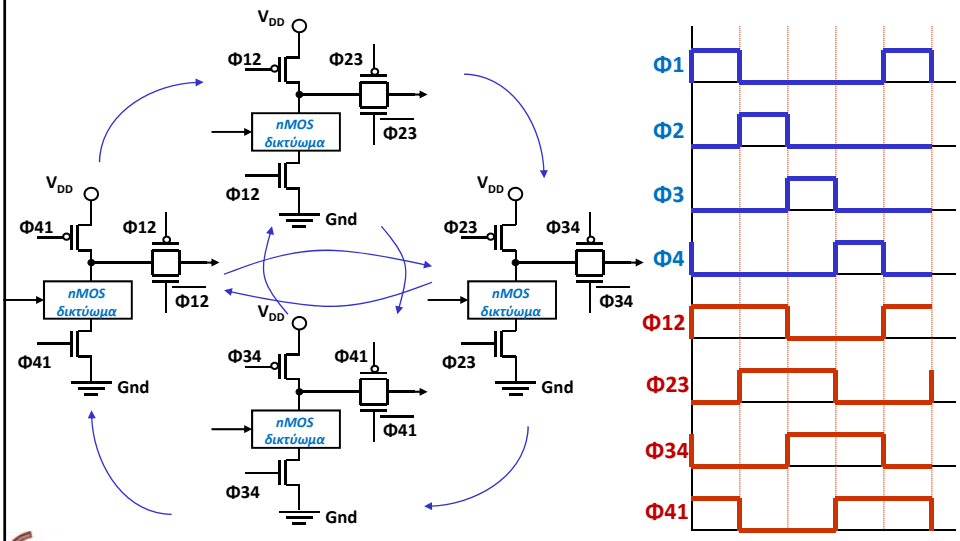


4 Phase Dynamic CMOS Logic I

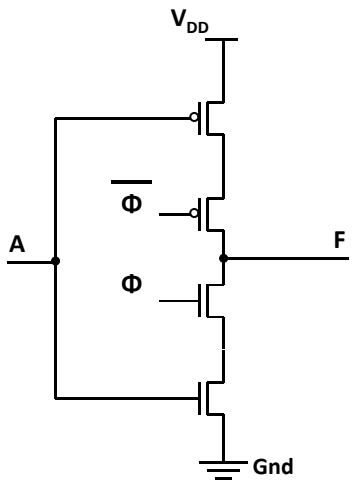


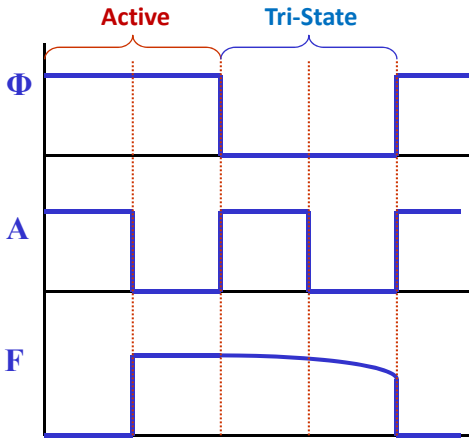


4 Phase Dynamic CMOS Logic II

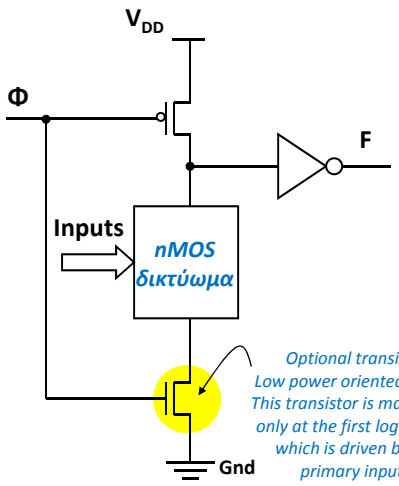


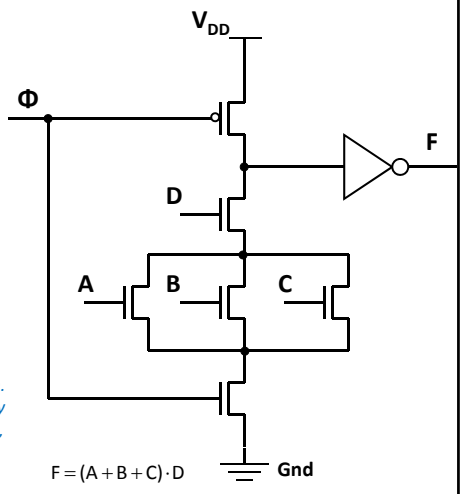
Clocked CMOS (C²MOS) Logic



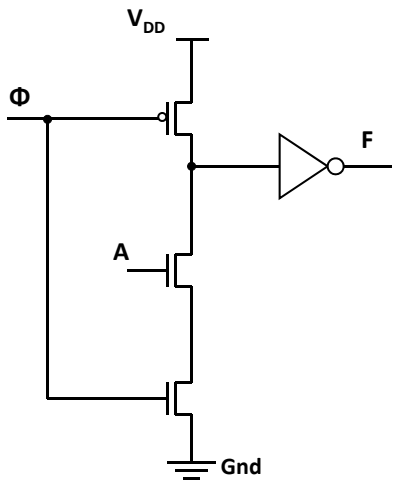


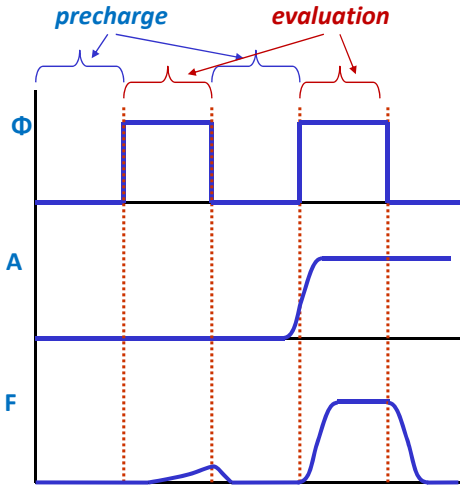
Domino CMOS Logic I



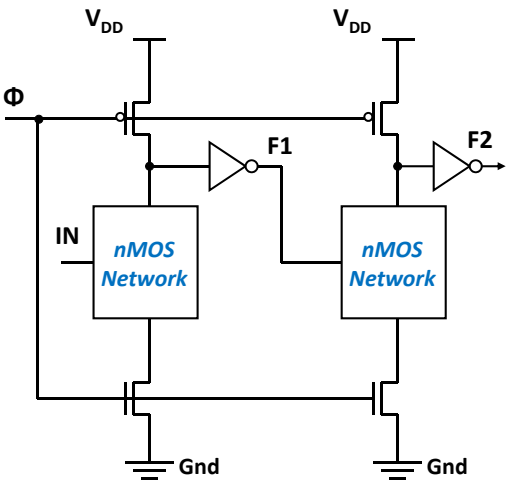


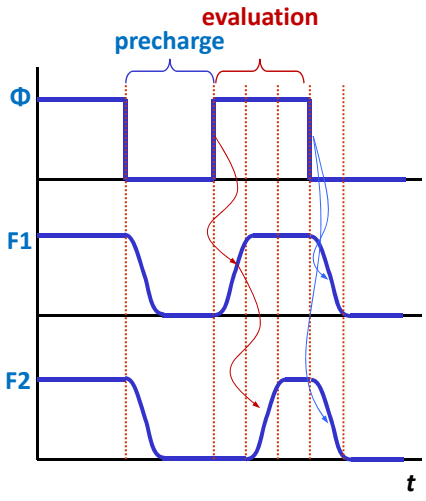
Domino CMOS Logic II





Domino CMOS Logic III

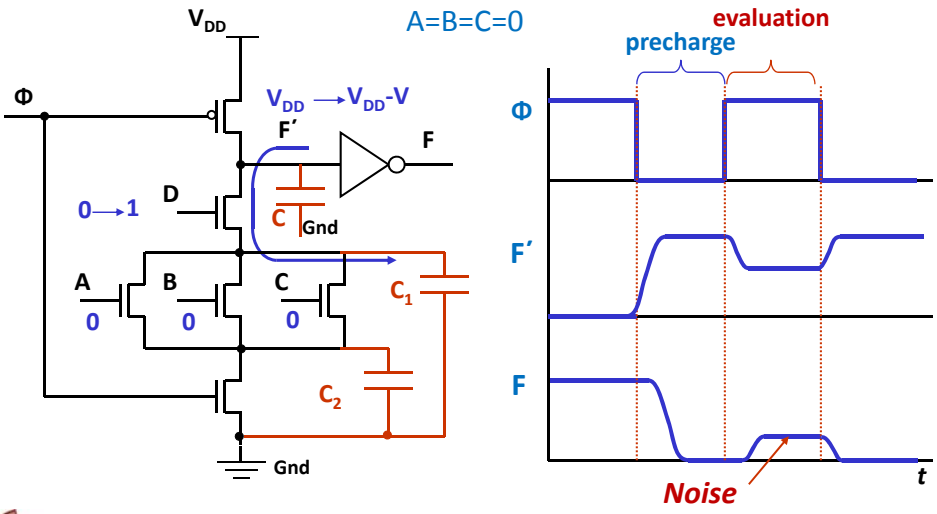




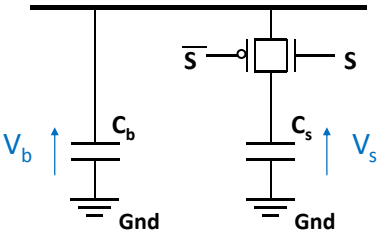
Domino CMOS Logic IV

Strengths	Weaknesses
Logic Density	Logically Incomplete Family
High Performance	Low Noise Immunity
Very Low Noise Generation	High Switch Factor
Non-Glitching Output	Limited Fail Diagnosability

Domino and Charge Sharing



Charge Sharing



S = '0' then:

$Q_b = C_b.V_b$ and $Q_s = C_s.V_s$

$Q_{total} = Q_b + Q_s = C_b.V_b + C_s.V_s$

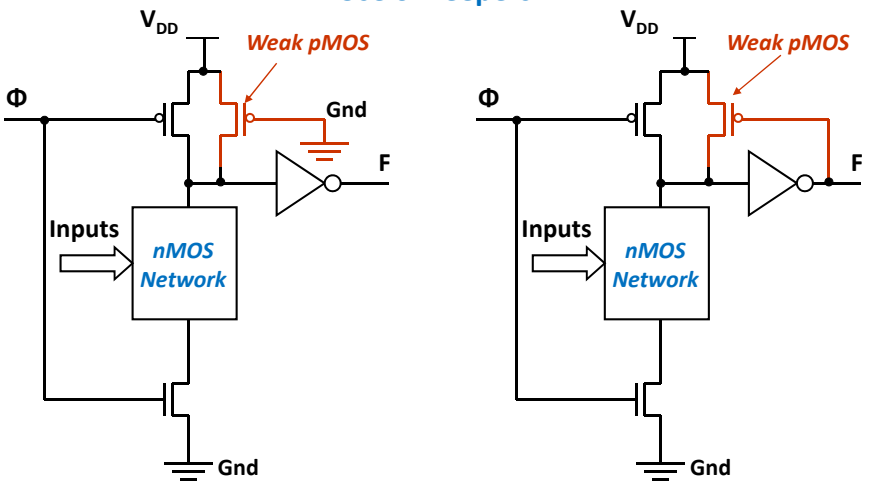
S = '1', then according to the charge retention principle:

$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_b V_b + C_s V_s}{C_b + C_s}$$

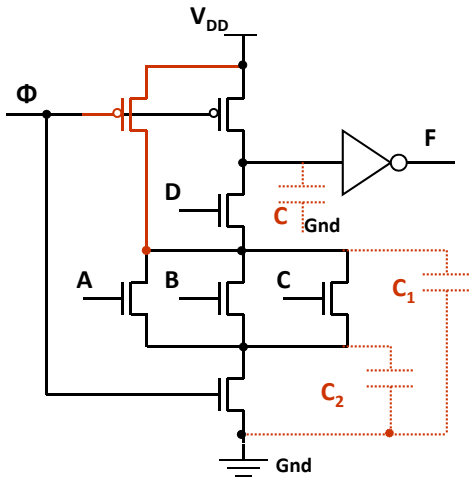
$C_{total} = C_b + C_s$

Enhanced Domino Logic

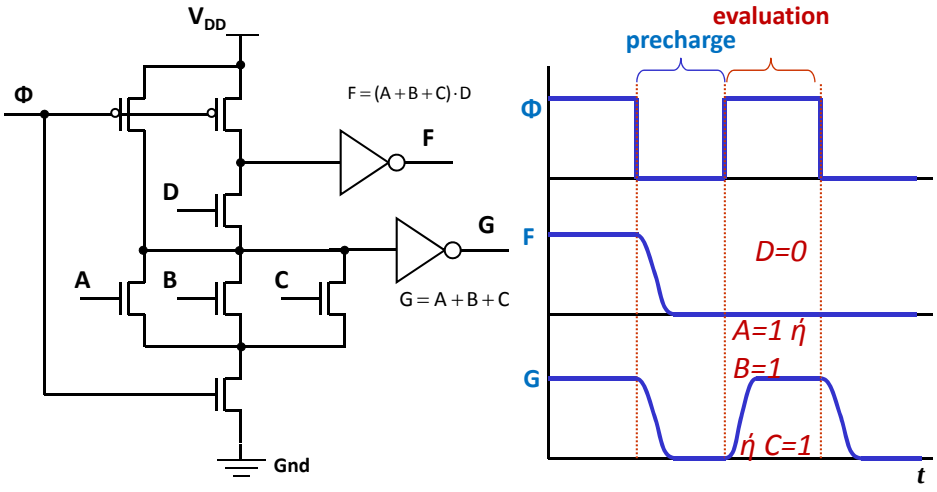
Use of keepers



Multiple Precharging Domino Logic



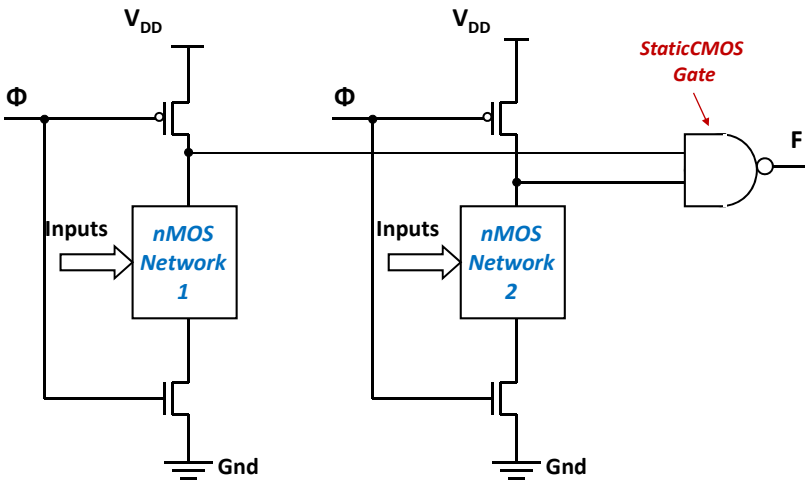
Multiple Output Domino Logic I



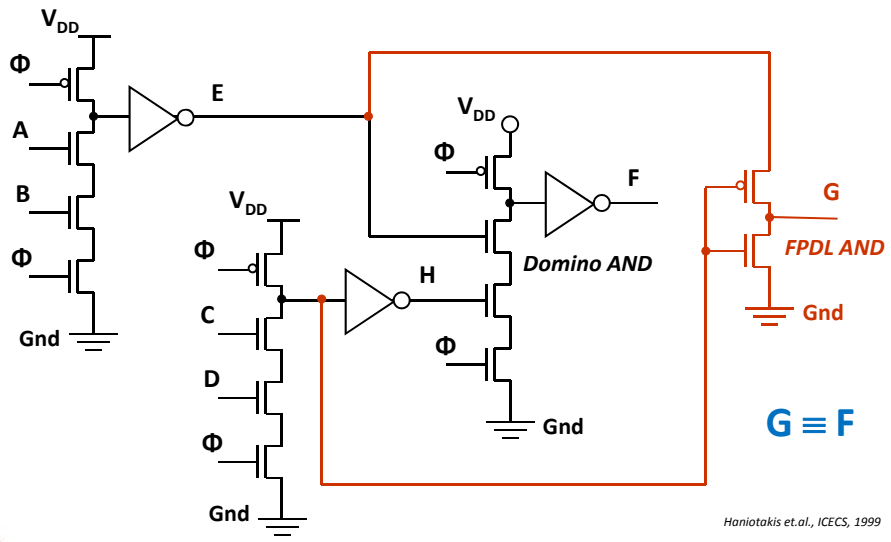
Multiple Output Domino Logic II

Strengths	Weaknesses
Active Power Reduction	Logically Incomplete Family
Area, Device Count Reduction	Large Evaluate Capacitance
Low Noise Generation	High Switching Factor
High Diagnosability	

Compound Domino Logic

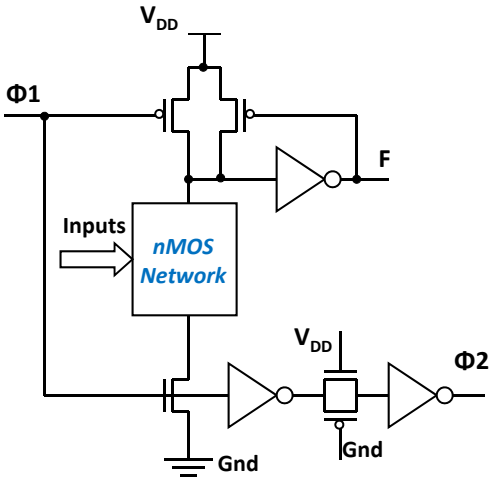


Clock-less Domino Logic Compatible Style



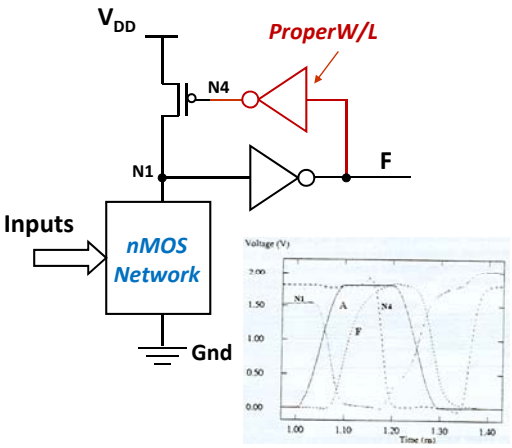
Haniotakis et.al., ICECS, 1999

Clock-Delayed Domino (CDD) Logic



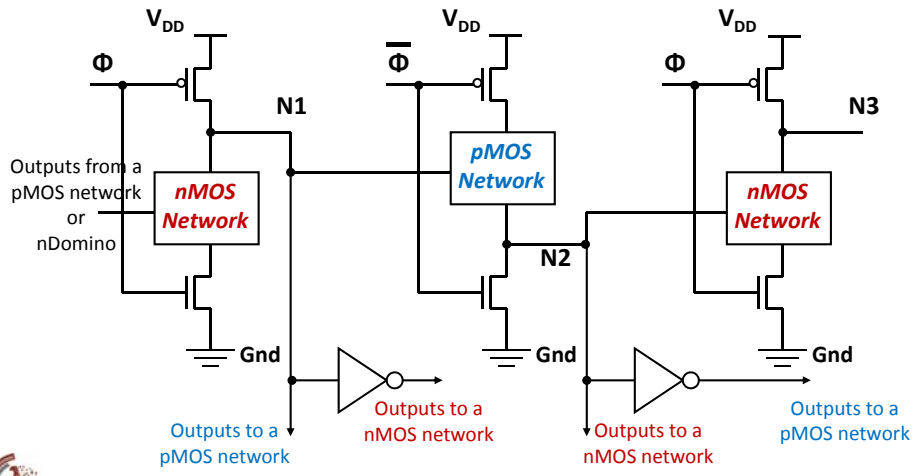
Strengths	Weaknesses
Logically Complete Family	Timing Complexity
Reduced Clock Overhead	Low Noise Immunity
	High Process Sensitivity
	Limited Fail Diagnosability
	Additional Clock Path

Self-Resetting Domino (SRD) Logic



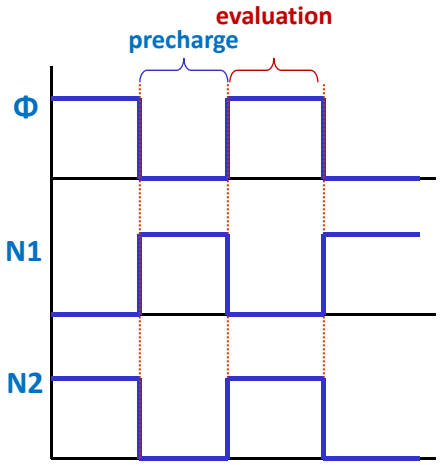
Strengths	Weaknesses
High Performance	Time Synchronization
Reduced Clock Overhead	Low Noise Immunity
Logically Complete Family	High Process Sensitivity
	Limited Fail Diagnosability
	Additional Device Count

No Race (NORA) Logic I



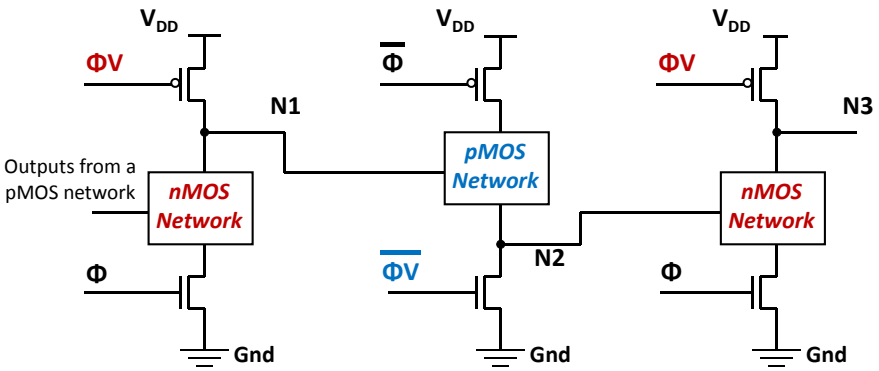
NORA Logic II

Strengths	Weaknesses
Reduced Delay Stages	pMOS Evaluation Devices
Low Fanout and Capacitance	Clocking Complexity
Low Area	Low Fanout Capability
Complete Logic Family	



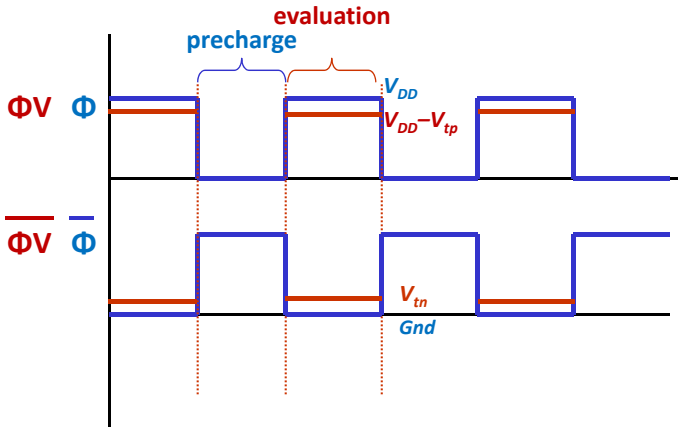
Zipper Domino Logic I

$\Phi V \in (0, V_{DD}-V_{tp})$

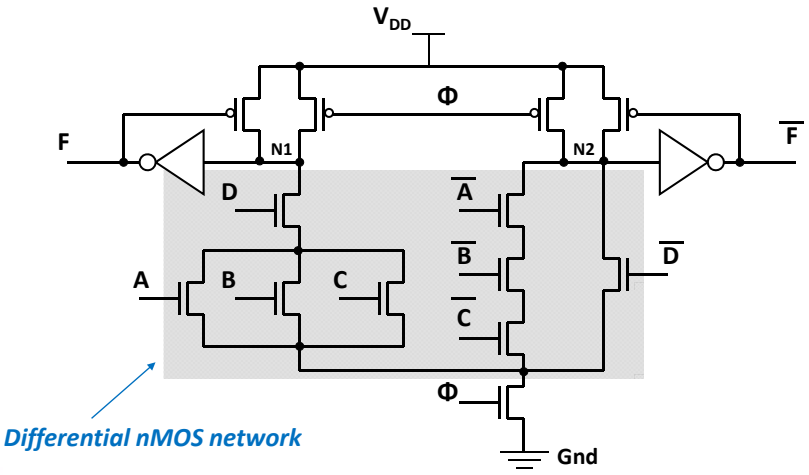


$\overline{\Phi V} \in (V_{tn}, V_{DD})$

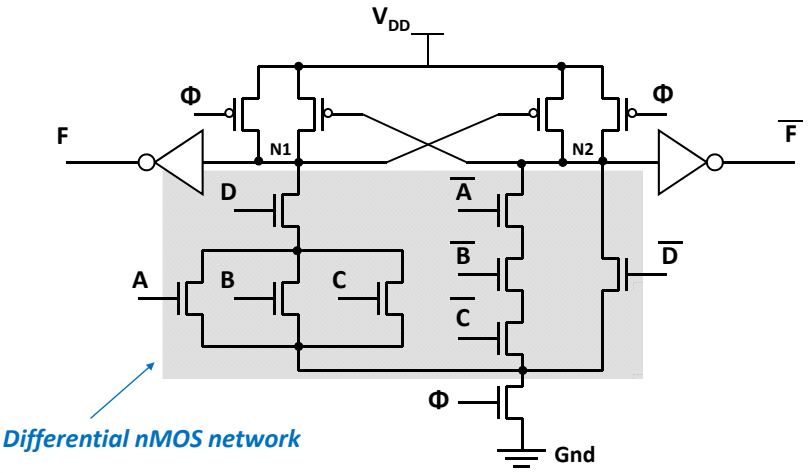
Zipper Domino Logic II



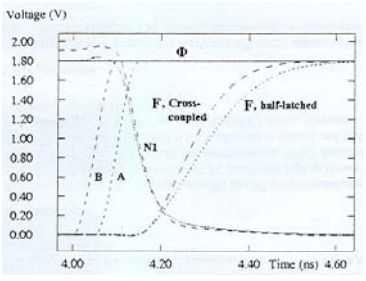
Differential Domino Logic (DDL)



Cross-Coupled Domino (CCD) Logic

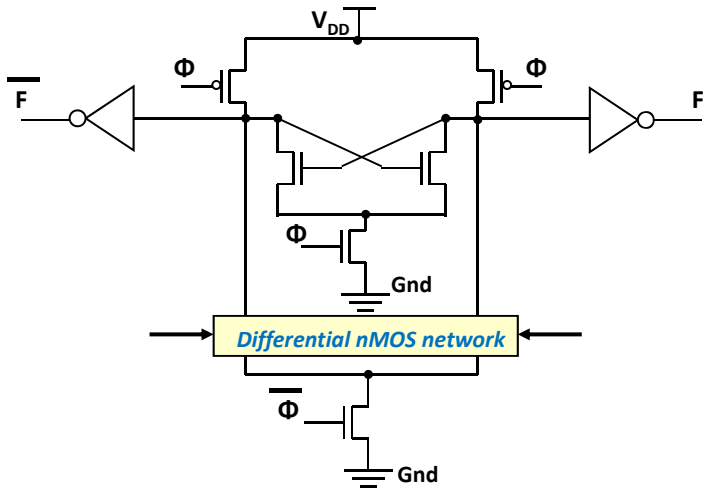


DDL and CCD Logic

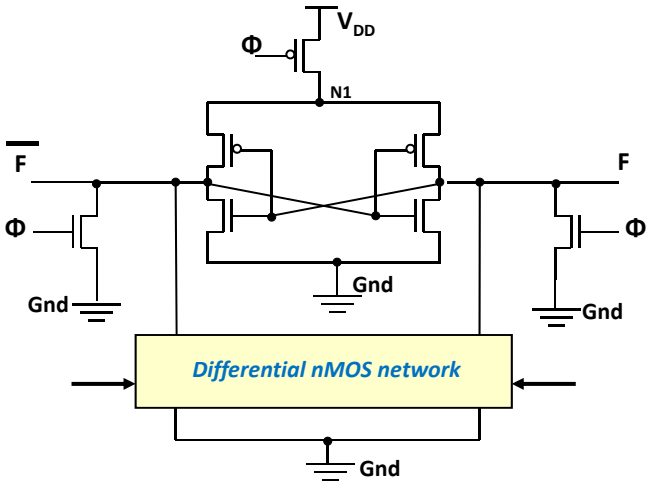


Strengths	Weaknesses
Logically Complete Family	High Device Count, Area
Enhanced Noise Immunity	High Clock Load
High Performance	High Power Consumption

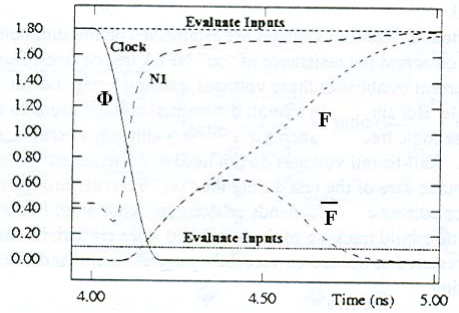
Sample-Set Differential (SSD) Logic



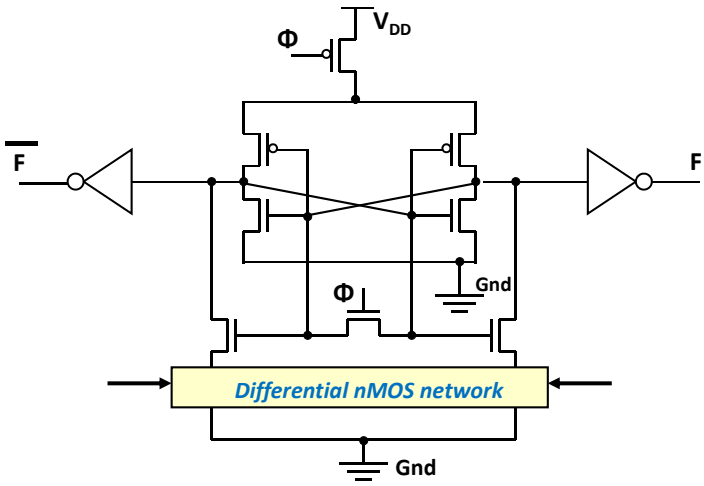
Enable-Disable CMOS Differential Logic (ECDL)



ECDL Logic



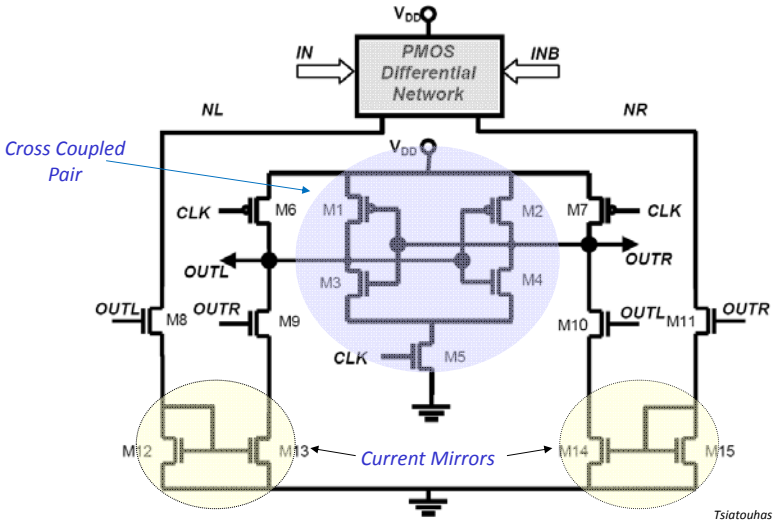
Differential Current Switch (DCS) Logic



SSD and DCS Logic

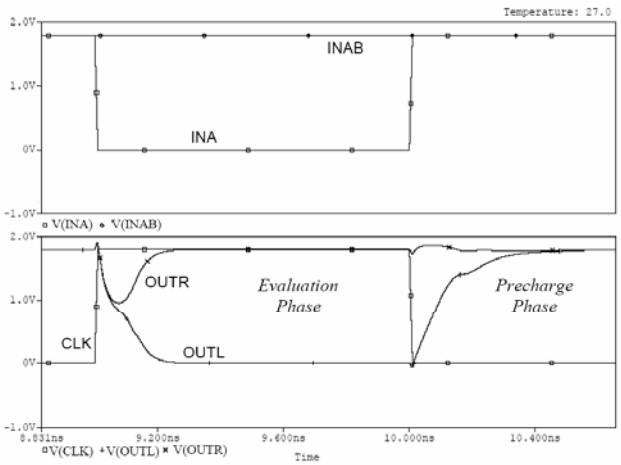
Strengths	Weaknesses
Logically Complete Family	High Device Count, Area
High Performance	High Clock Load, Routing
High Logic Depth	Clock Generation Constrains

Differential Current Mirror (DCM) Logic I

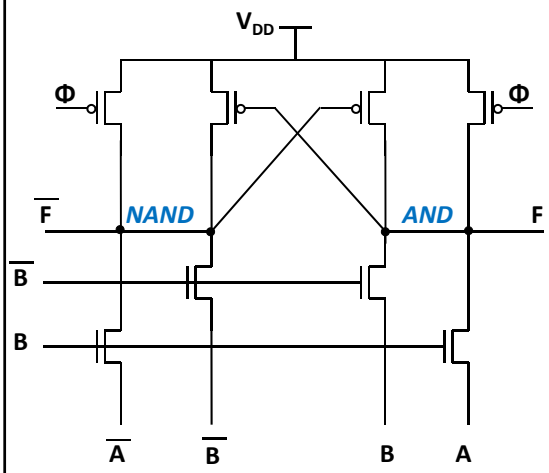


Tsiatouhas et.al., ISCAS, 2006

Differential Current Mirror (DCM) Logic II



Dynamic Complementary Pass Gate (DCP) Logic



Strengths	Weaknesses
nMOS Evaluation	Complementary I/O Needed
Glitch-Free Operation	Charge Redistribution
	Added Clock Load

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