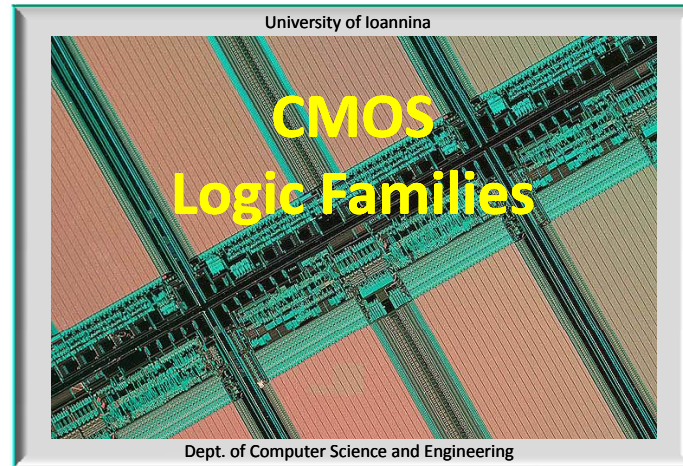


CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES



Y. Tsiatouhas



CMOS Integrated Circuit Design Techniques



Overview

- 1. Non-clocked CMOS logic families*
- 2. Clocked CMOS logic families*



VLSI Systems
and Computer Architecture Lab

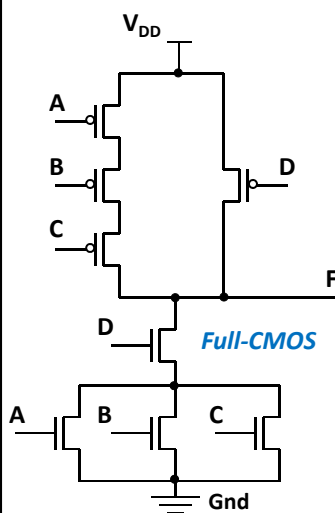
Non-Clocked CMOS Logic Families



CMOS Logic Families

3

Full or Static CMOS Logic



$$F = \overline{((A + B + C) \cdot D)}$$

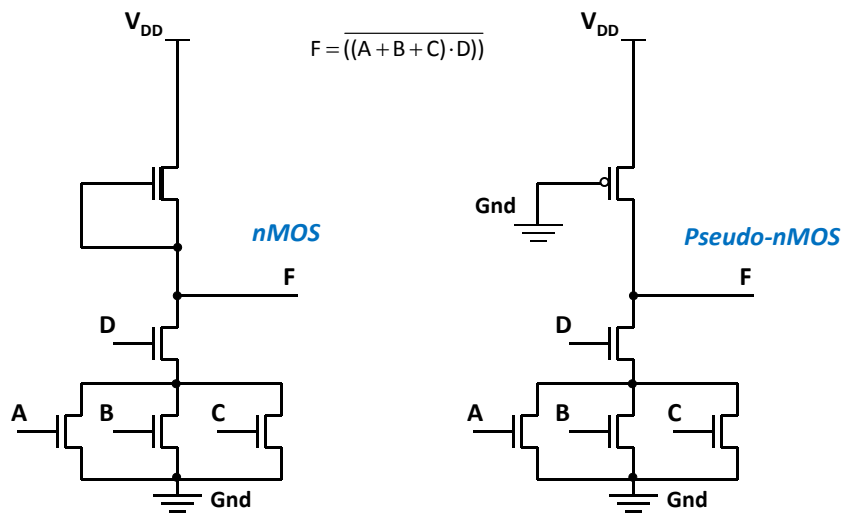
Strengths	Weaknesses
Low Static Power	Overlap Currents
Good Yield/Defect Tolerance	High Fan-Out Loads
High Test Coverage	High Noise Generation
High Noise Immunity	



CMOS Logic Families

4

nMOS and Pseudo-nMOS Logic

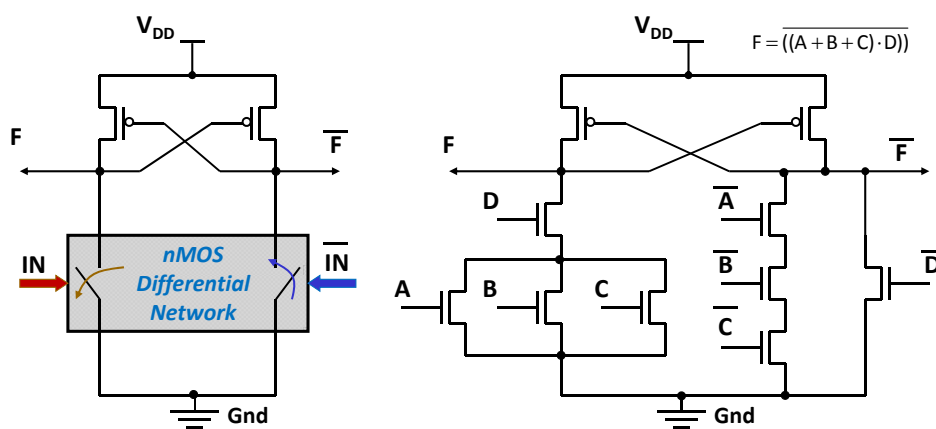


CMOS Logic Families

5

Differential Cascode Voltage Switch Logic I

DCVS



CMOS Logic Families

6

DCVS Logic II

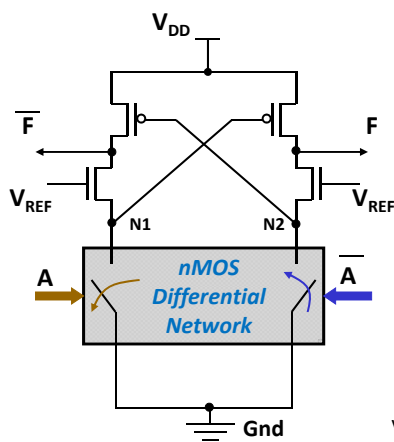
Strengths	Weaknesses
Good Logic Density	Dual Rail Wiring
Complementary Output Availability	pMOS Strength vs Latching Hysteresis
High Reliability	High Device Count (depending on applic.)
High Noise Immunity	



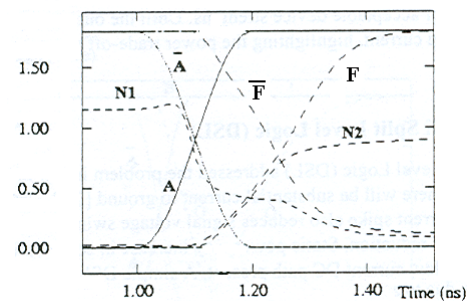
CMOS Logic Families

7

Differential Split-Level (DSL) Logic I



Voltage (Volts)



$$V_{REF} = \frac{V_{DD}}{2} + V_{tn}$$



CMOS Logic Families

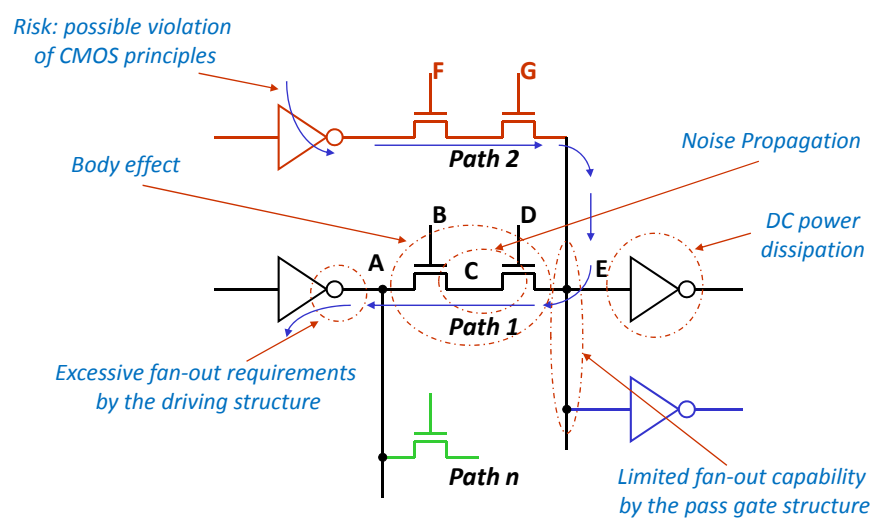
8

DSL Logic II

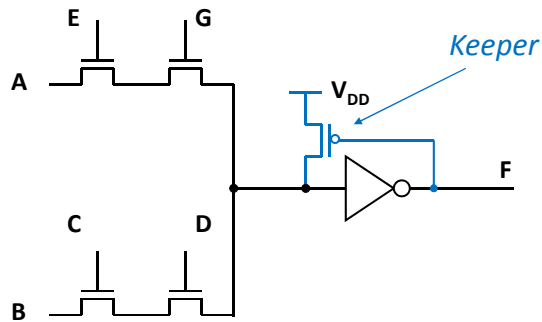
Strengths	Weaknesses
Low Switching Power Dissipation	High Static Power Dissipation
Complementary Output Availability	V_{REF} Generation
High Reliability	High Device Count



Pass Gate Logic



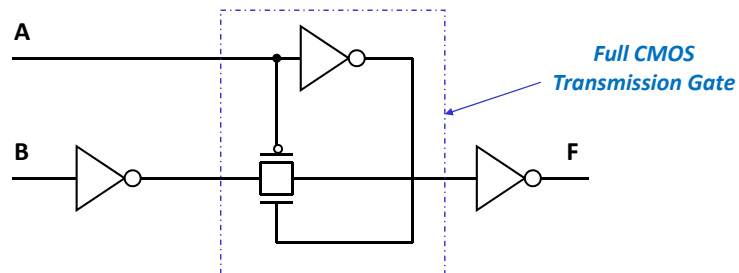
Keeper Based Pass Gate Logic



CMOS Logic Families

11

Full CMOS Transmission Gate Logic



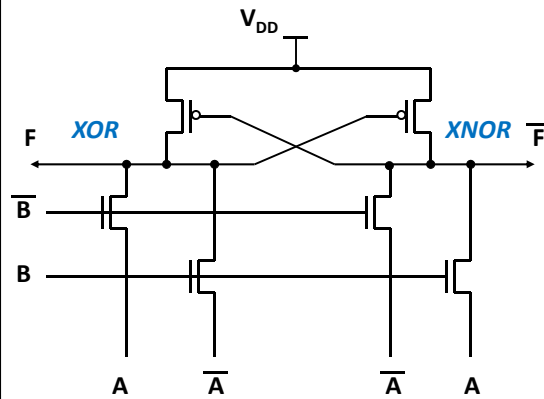
Strengths	Weaknesses
High Speed	Body Effect
Low Area	Limited Logic Depth
Low Power	



CMOS Logic Families

12

DCVS Logic with Pass Gates



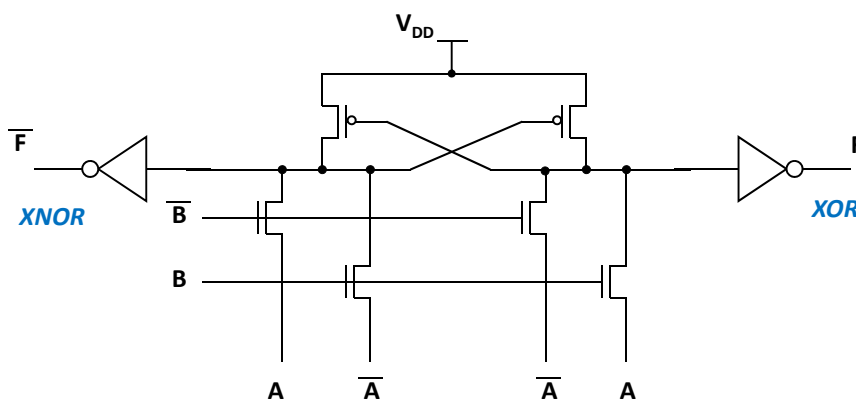
Strengths	Weaknesses
Full Swing	Limited Logic Depth
Noise Immunity	Limited Load Drive
Area-Power Reduction	Body Effect
No Floating Nodes	



CMOS Logic Families

13

Complementary Pass Gate Logic (CPL)



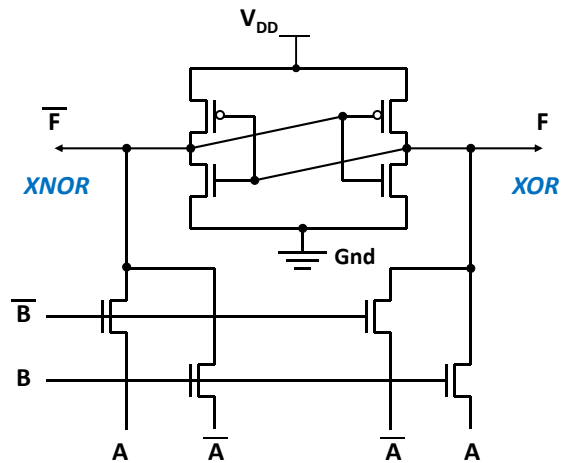
High Speed Operation



CMOS Logic Families

14

Swing-Restored Pass Gate Logic (SRPL) I



CMOS Logic Families

15

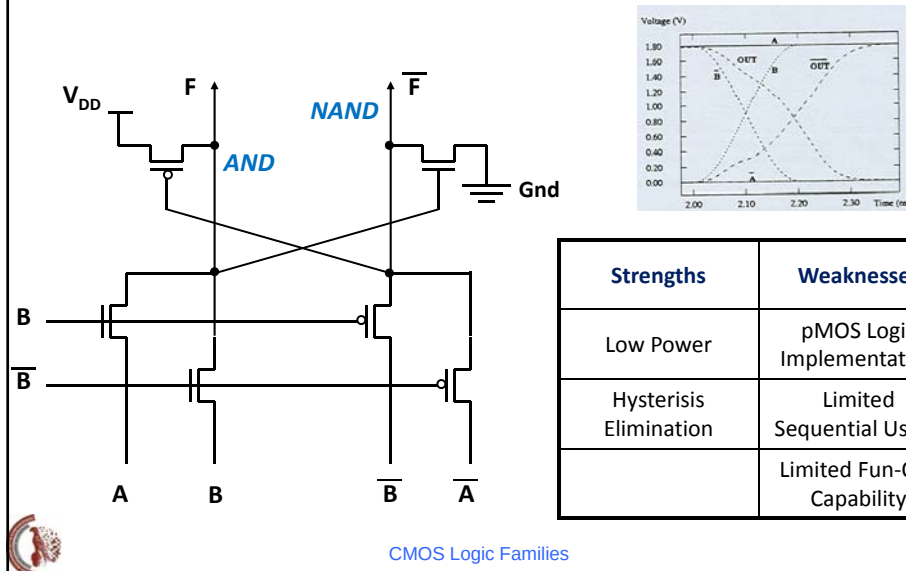
SRPL Logic II

Strengths	Weaknesses
Low Static Power Dissipation	Limited Output Load
Process Tolerance	Overlapping Current
Sense Amplifier Speed Performance	Drive Strength vs Performance
High Logic Depth	

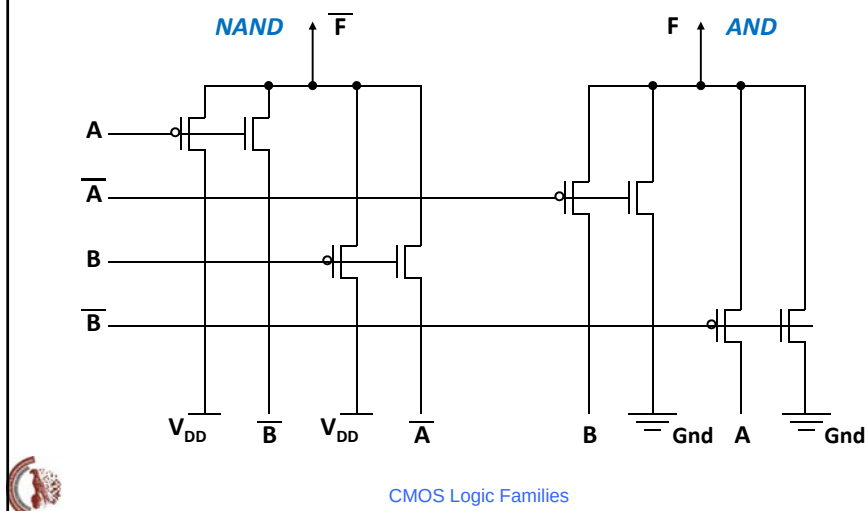
CMOS Logic Families

16

Push-Pull Pass Transistor Logic (PPL)



Double Pass Transistor Logic (DPL) I



DPL Logic II

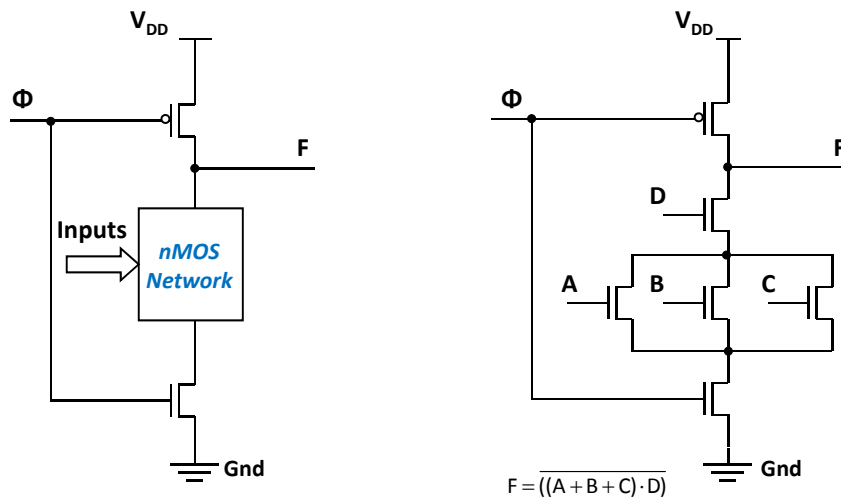
Strengths	Weaknesses
High Speed Operation	Limited Logic Depth
No V_{th} Drops	Limited Load Capability
	Redundant Device Structure



Clocked CMOS Logic Families



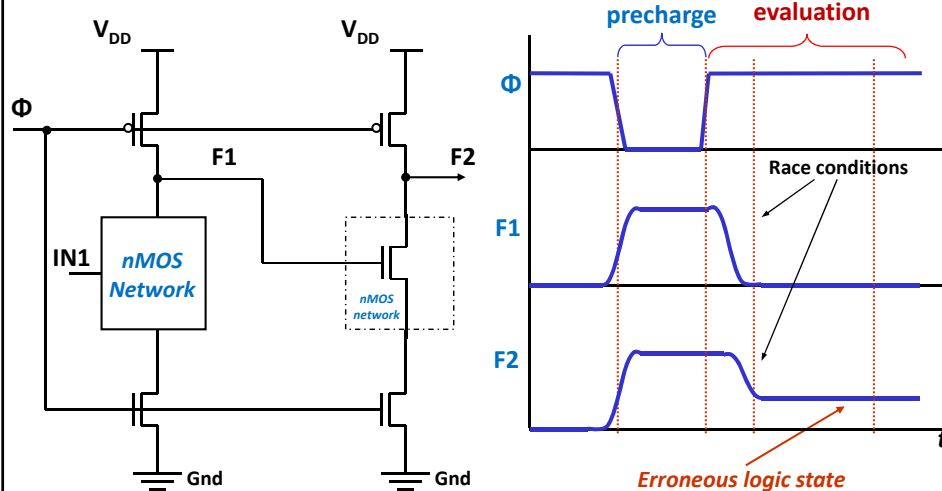
Dynamic CMOS Logic I



CMOS Logic Families

21

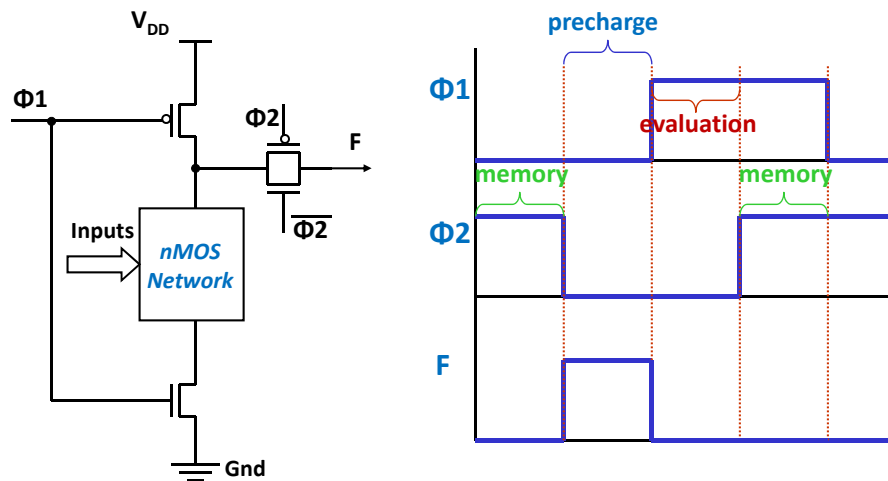
Dynamic CMOS Logic II



CMOS Logic Families

22

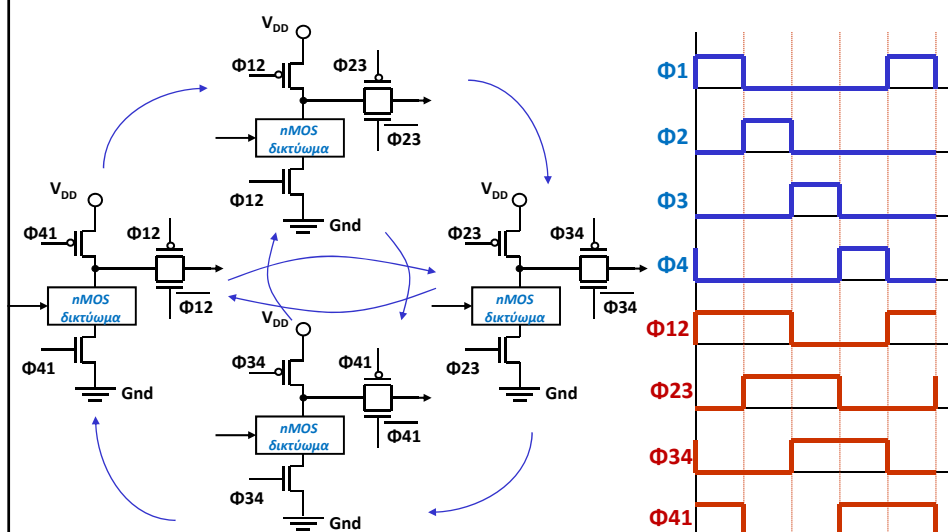
4 Phase Dynamic CMOS Logic I



CMOS Logic Families

23

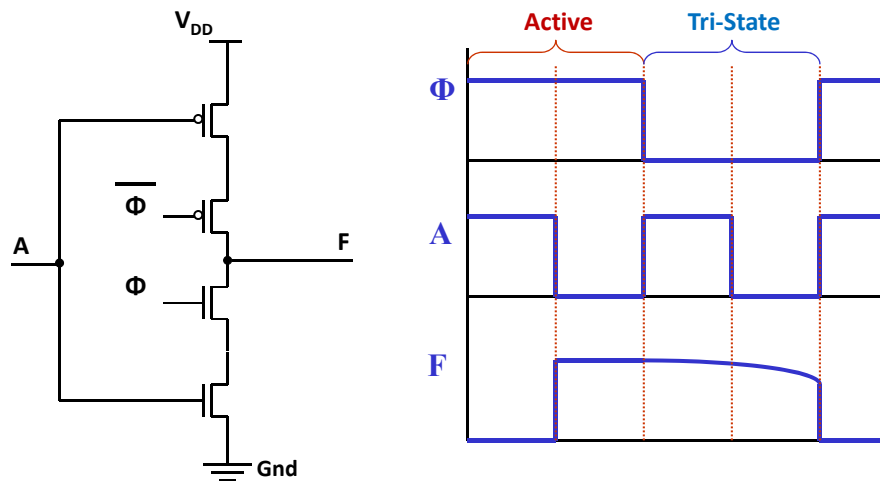
4 Phase Dynamic CMOS Logic II



CMOS Logic Families

24

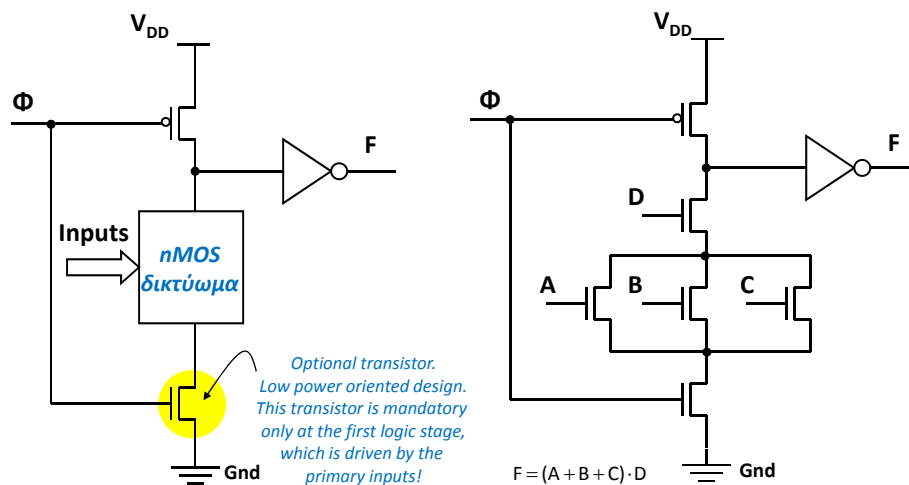
Clocked CMOS (C²MOS) Logic



CMOS Logic Families

25

Domino CMOS Logic I



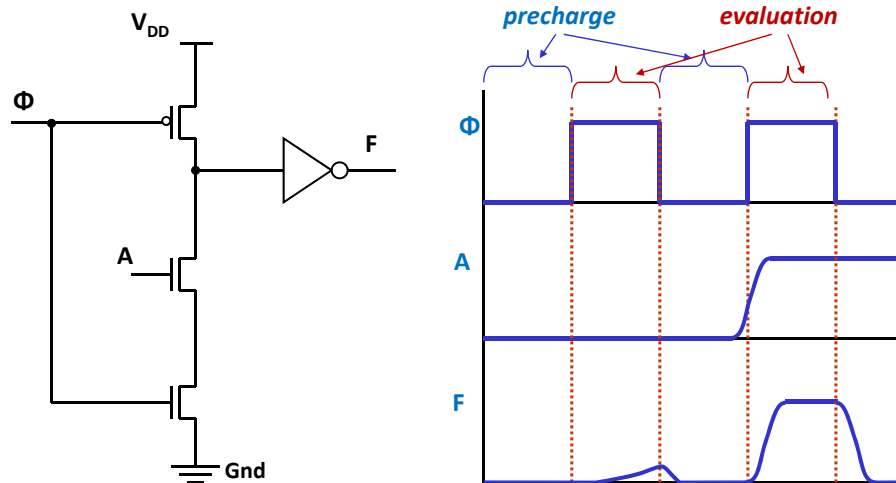
*Optional transistor.
Low power oriented design.
This transistor is mandatory
only at the first logic stage,
which is driven by the
primary inputs!*

$$F = (A + B + C) \cdot D$$

CMOS Logic Families

26

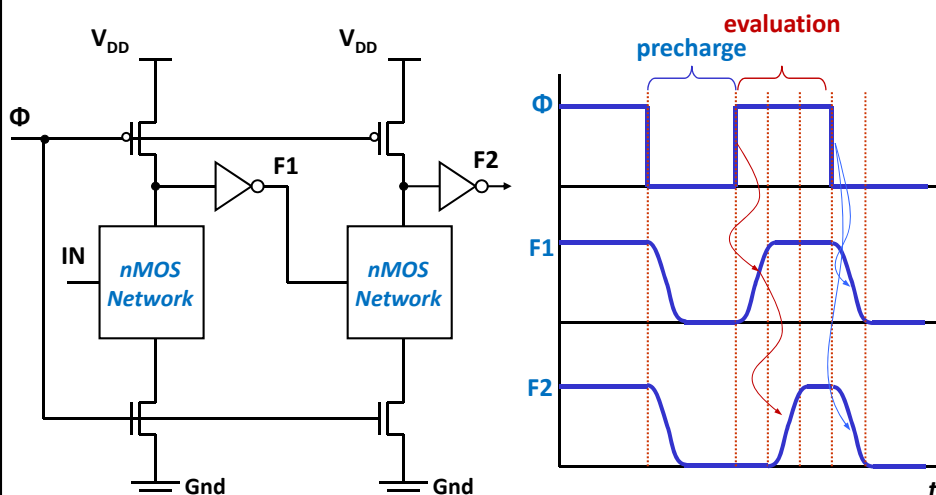
Domino CMOS Logic II



CMOS Logic Families

27

Domino CMOS Logic III



CMOS Logic Families

28

Domino CMOS Logic IV

Strengths	Weaknesses
Logic Density	Logically Incomplete Family
High Performance	Low Noise Immunity
Very Low Noise Generation	High Switch Factor
Non-Glitching Output	Limited Fail Diagnosability

CMOS Logic Families

29

Domino and Charge Sharing

The circuit diagram on the left shows a Domino and Charge Sharing circuit. It consists of a PMOS transistor at the top connected to V_{DD} and a network of NMOS transistors at the bottom connected to ground. The NMOS network has three parallel branches: a left branch with NMOS A, a middle branch with NMOS B and C in series, and a right branch with NMOS C. Input A is labeled with a blue '0' and a blue arrow pointing to '1'. Input B is labeled with a blue '0'. Input C is labeled with a blue '0'. The output node F' is connected to a PMOS transistor and a node F through an inverter. A capacitor C is connected between F' and ground. A blue arrow indicates a signal transition from 0 to 1 at input A. A red arrow points to the output F, which is labeled 'Noise'. The timing diagram on the right shows the waveforms for Φ , F', and F over time t. The clock Φ has two phases: precharge (blue) and evaluation (red). During precharge, F' is high and F is low. During evaluation, F' is low and F is high. A red arrow points to a small spike in the F waveform during the evaluation phase, labeled 'Noise'.

Domino and Charge Sharing

$A=B=C=0$

V_{DD}

Φ

$V_{DD} \rightarrow V_{DD}-V$

F'

F

D

$0 \rightarrow 1$

A

B

C

0

0

0

C_1

C_2

Gnd

precharge

evaluation

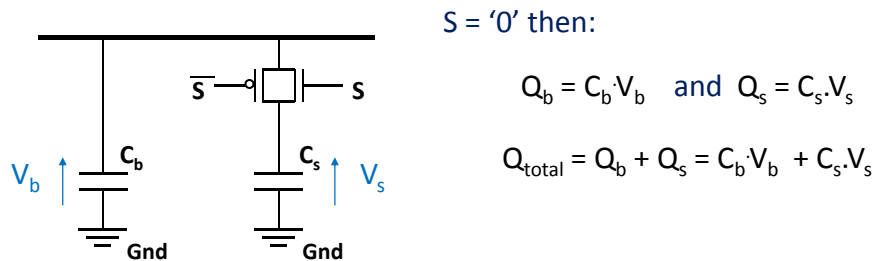
Noise

t

CMOS Logic Families

30

Charge Sharing



$S = '1'$, then according to the charge retention principle:

$$V_R = \frac{Q_{total}}{C_{total}} = \frac{C_b V_b + C_s V_s}{C_b + C_s}$$

$$C_{total} = C_b + C_s$$

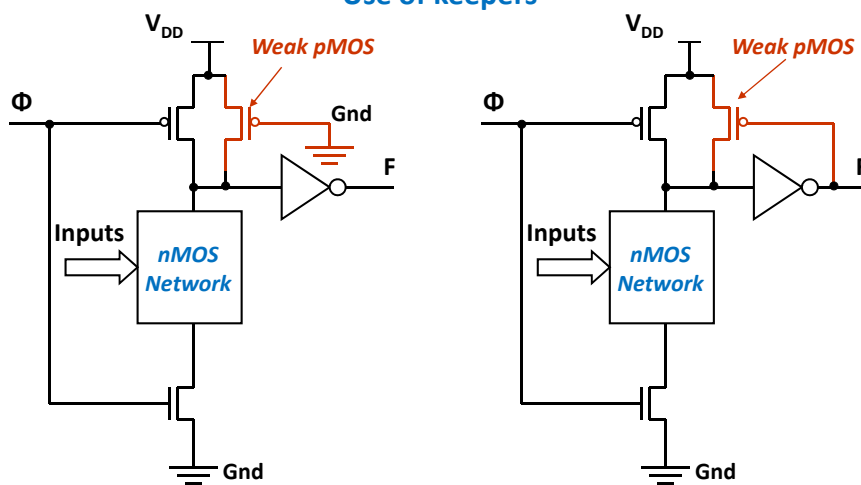


CMOS Logic Families

31

Enhanced Domino Logic

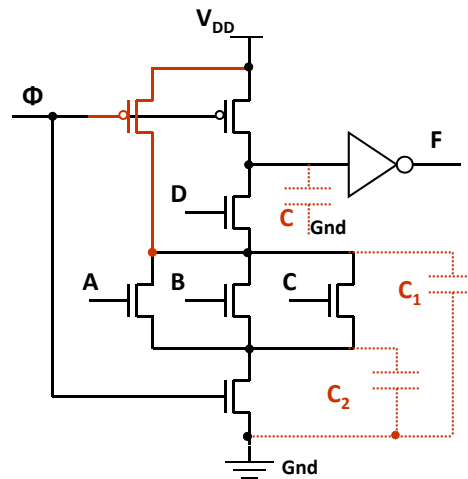
Use of keepers



CMOS Logic Families

32

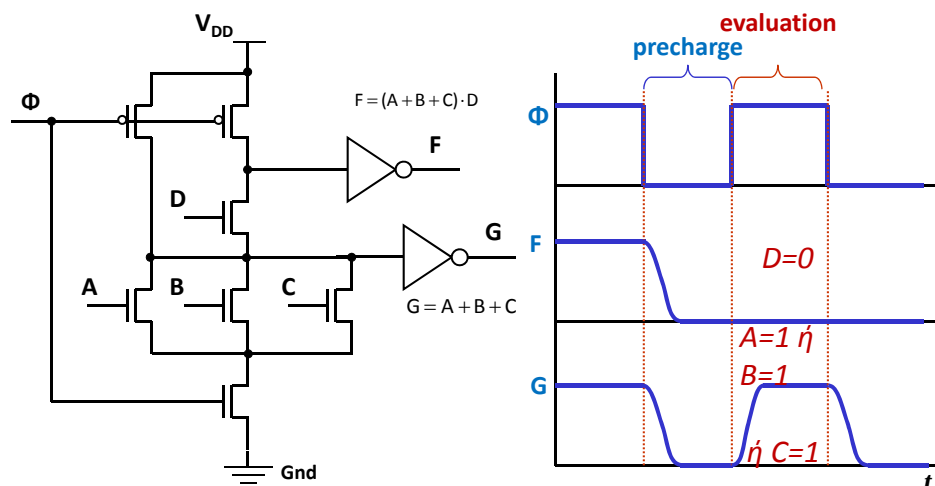
Multiple Precharging Domino Logic



CMOS Logic Families

33

Multiple Output Domino Logic I



CMOS Logic Families

34

Multiple Output Domino Logic II

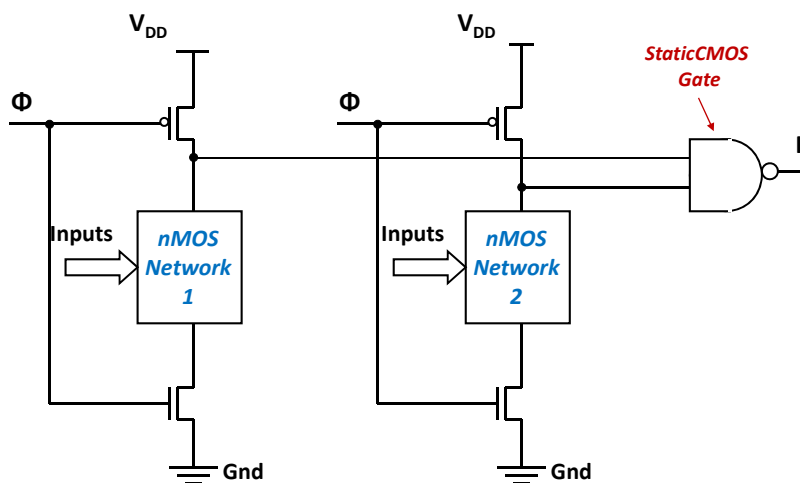
Strengths	Weaknesses
Active Power Reduction	Logically Incomplete Family
Area, Device Count Reduction	Large Evaluate Capacitance
Low Noise Generation	High Switching Factor
High Diagnosability	



CMOS Logic Families

35

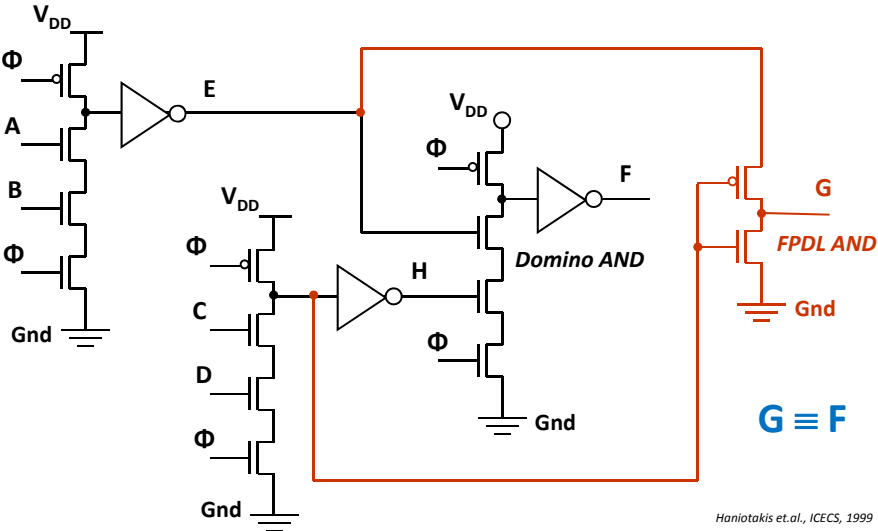
Compound Domino Logic



CMOS Logic Families

36

Clock-less Domino Logic Compatible Style

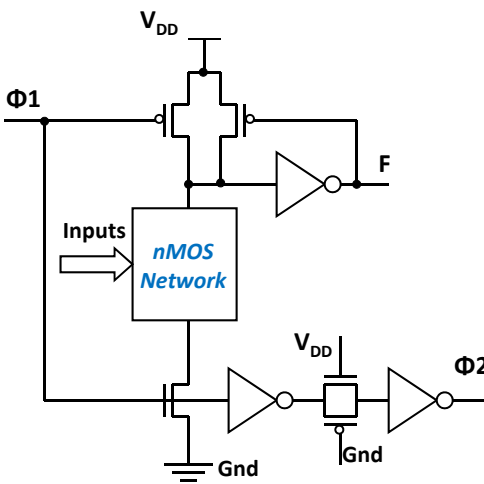


Haniotakis et.al., ICECS, 1999

CMOS Logic Families

37

Clock-Delayed Domino (CDD) Logic

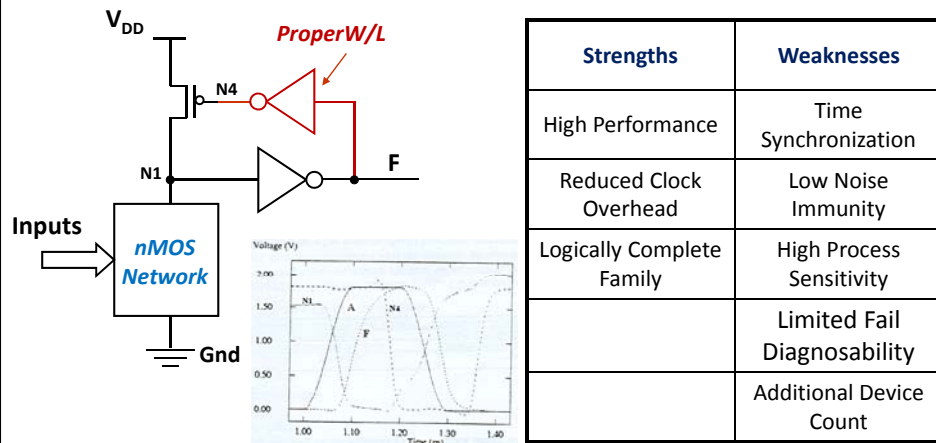


Strengths	Weaknesses
Logically Complete Family	Timing Complexity
Reduced Clock Overhead	Low Noise Immunity
	High Process Sensitivity
	Limited Fail Diagnosability
	Additional Clock Path

CMOS Logic Families

38

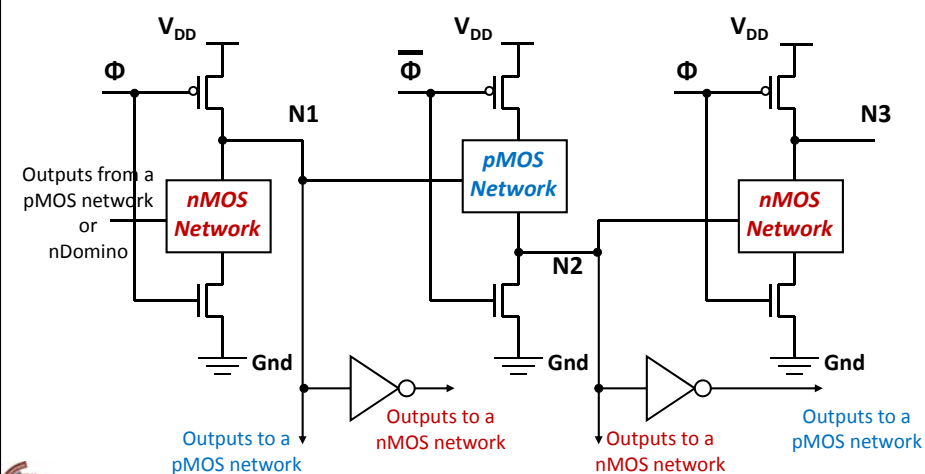
Self-Resetting Domino (SRD) Logic



CMOS Logic Families

39

No Race (NORA) Logic I

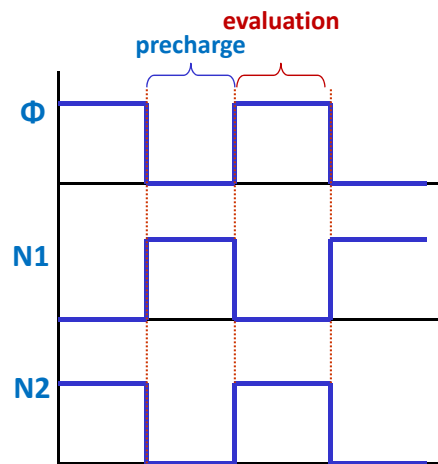


CMOS Logic Families

40

NORA Logic II

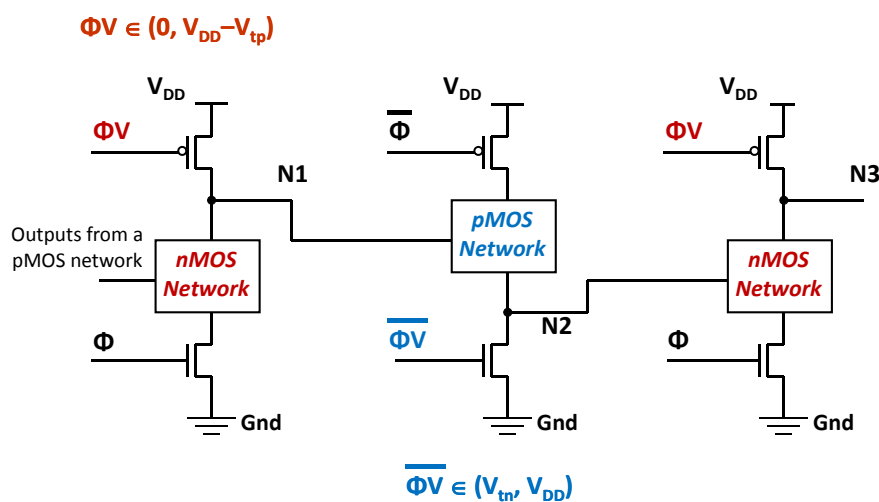
Strengths	Weaknesses
Reduced Delay Stages	pMOS Evaluation Devices
Low Fanout and Capacitance	Clocking Complexity
Low Area	Low Fanout Capability
Complete Logic Family	



CMOS Logic Families

41

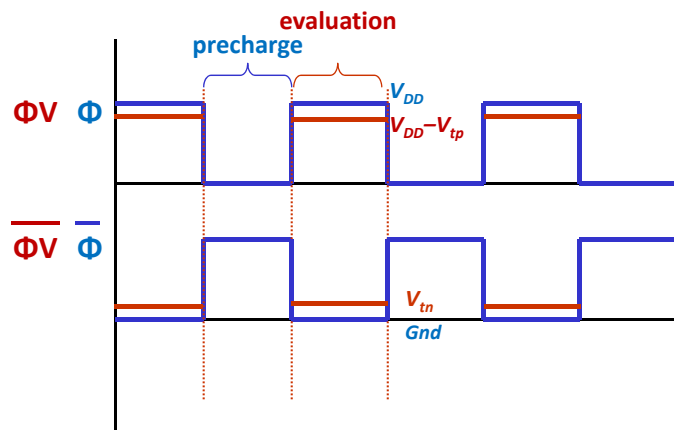
Zipper Domino Logic I



CMOS Logic Families

42

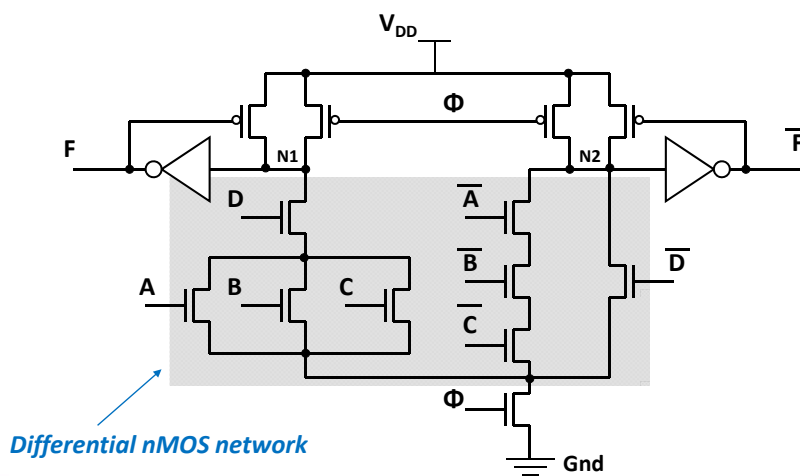
Zipper Domino Logic II



CMOS Logic Families

43

Differential Domino Logic (DDL)

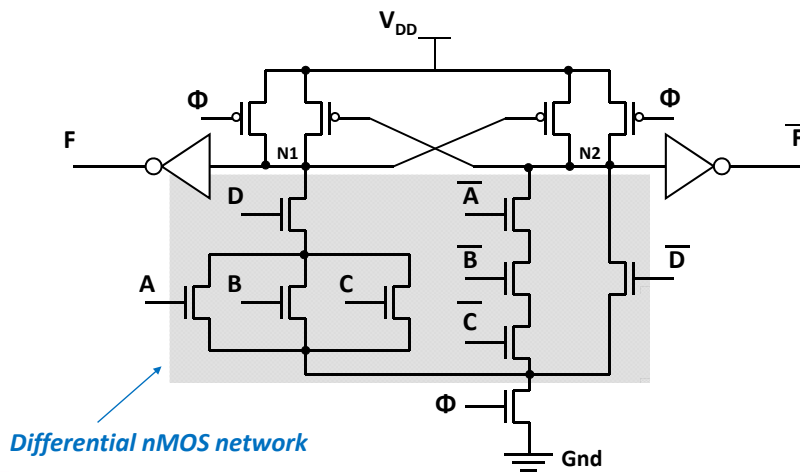


Differential nMOS network

CMOS Logic Families

44

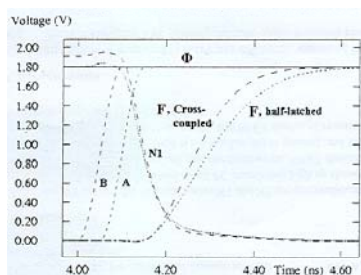
Cross-Coupled Domino (CCD) Logic



CMOS Logic Families

45

DDL and CCD Logic

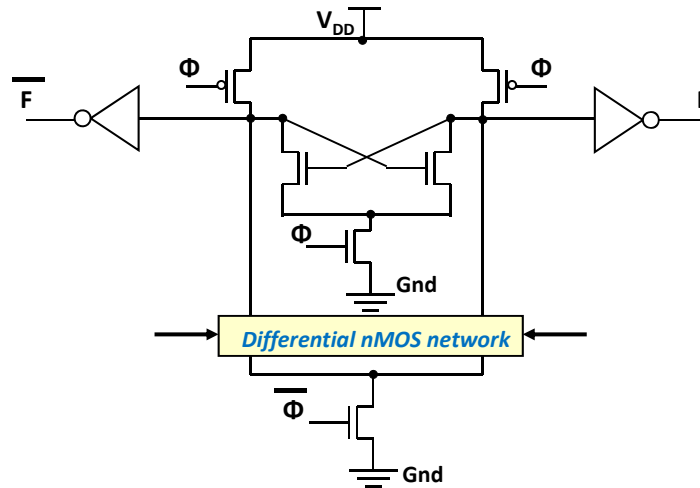


Strengths	Weaknesses
Logically Complete Family	High Device Count, Area
Enhanced Noise Immunity	High Clock Load
High Performance	High Power Consumption

CMOS Logic Families

46

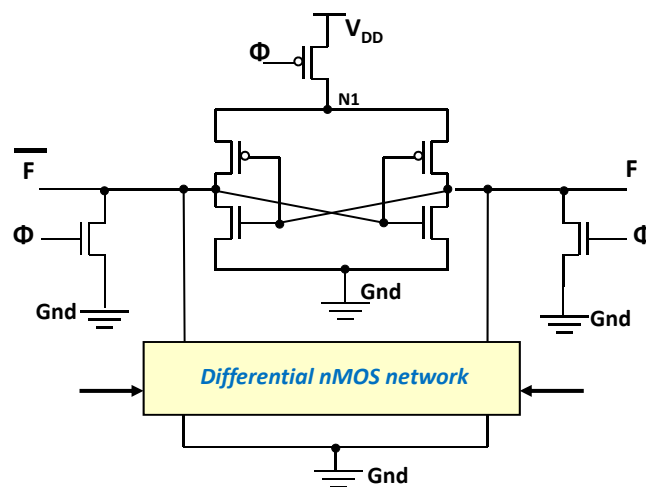
Sample-Set Differential (SSD) Logic



CMOS Logic Families

47

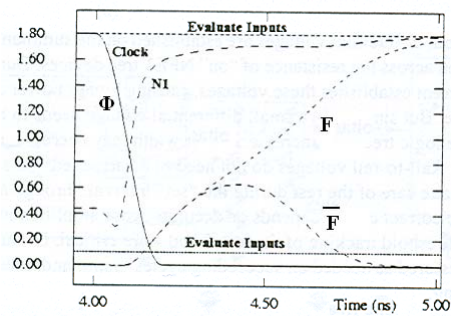
Enable-Disable CMOS Differential Logic (ECDL)



CMOS Logic Families

48

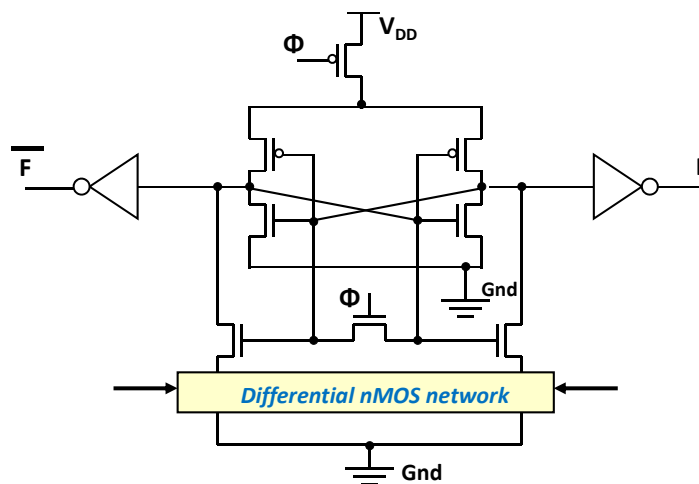
ECDL Logic



CMOS Logic Families

49

Differential Current Switch (DCS) Logic



CMOS Logic Families

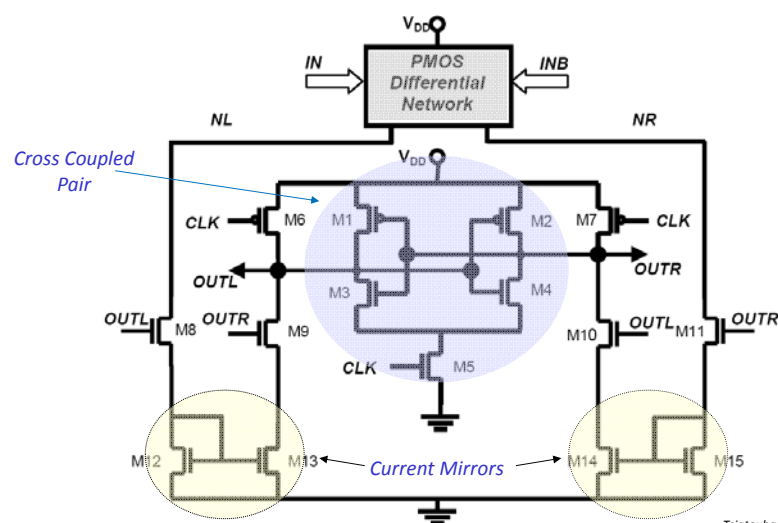
50

SSD and DCS Logic

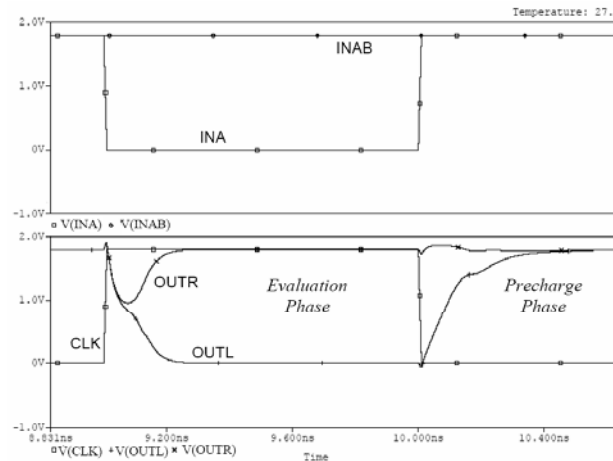
Strengths	Weaknesses
Logically Complete Family	High Device Count, Area
High Performance	High Clock Load, Routing
High Logic Depth	Clock Generation Constrains



Differential Current Mirror (DCM) Logic I



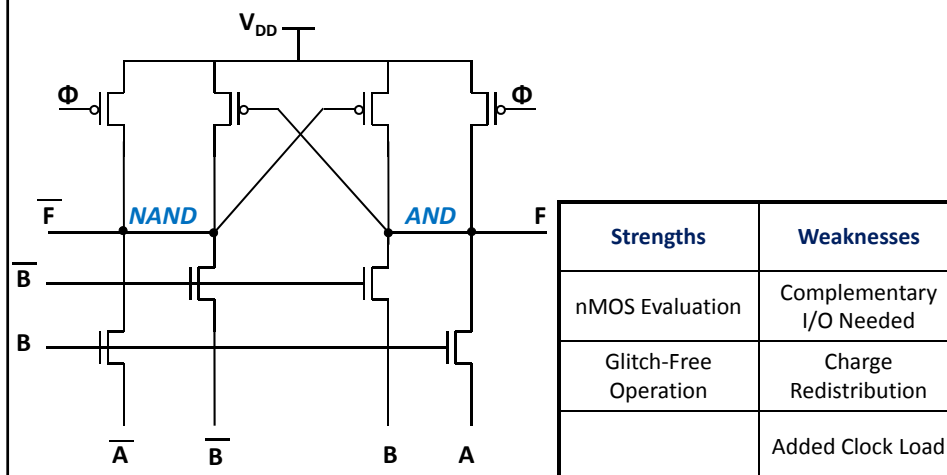
Differential Current Mirror (DCM) Logic II



CMOS Logic Families

53

Dynamic Complementary Pass Gate (DCP) Logic



CMOS Logic Families

54

Bibliography

- *“High Speed CMOS Design Styles,”* K. Bernstein, K. Carring, C. Durham, P. Hansen, D. Hogenmiller, E. Nowak and N. Rohrer, Kluwer, 6th Edition, 2002.
- *“Digital Integrated Circuits: A Design Perspective,”* J. Rabaey, A. Chandrakasan and B. Nikoloc, Prentice Hall, 2003.
- *“Design of High-Performance Microprocessor Circuits,”* A. Chandrakasan, W. Bowhill and F. Fox, IEEE Press, 2001.

