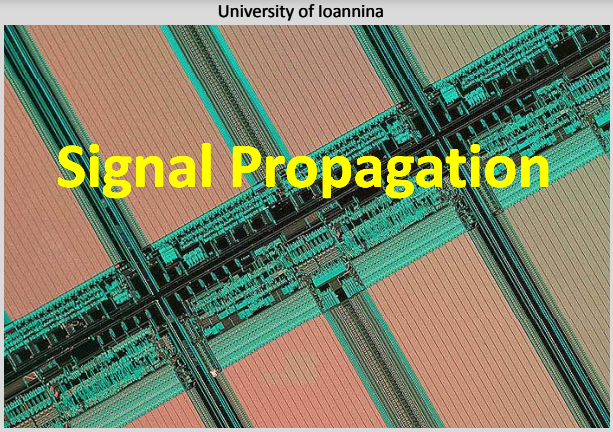
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

University of Ioannina



Dept. of Computer Science and Engineering

Survey on CMOS Digital Circuits

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CMOS Integrated Circuit Design Techniques

Overview

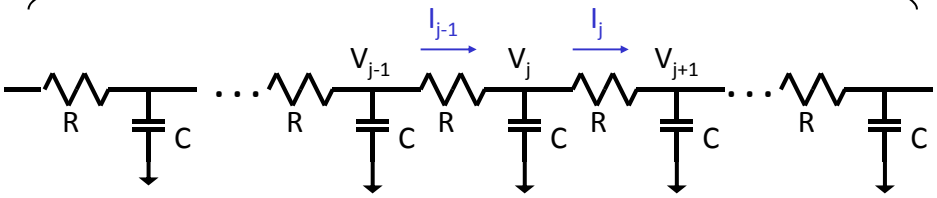
1. *Wire delay*
2. *Gate delay*
3. *Miller effect*
4. *Feed-forward*
5. *Negative resistance – capacitance*

VLSI Systems
and Computer Architecture Lab

Wire Delay

Distributed RC Model I

n – stages, total length ℓ



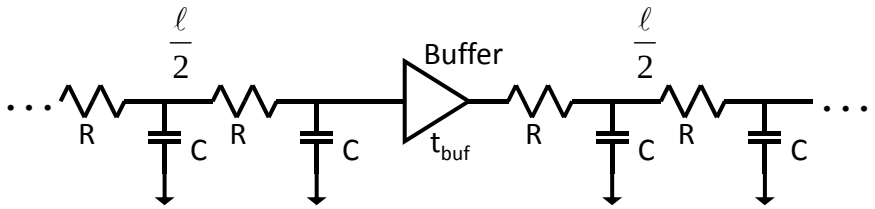
When n>>> the signal propagation delay time is given by:

$$t_p = \frac{rc\ell^2}{2}$$

Elmore Equation

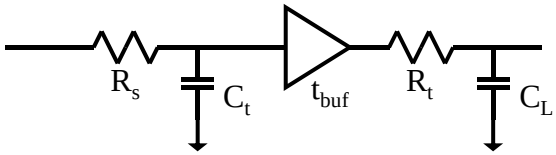
Where: r is the resistance/unit length, c is the capacitance/unit length and ℓ the wire length

Distributed RC Model II



$$t_p = t_{pl1} + t_{buf} + t_{pl2} = \frac{rc\left(\frac{\ell}{2}\right)^2}{2} + t_{buf} + \frac{rc\left(\frac{\ell}{2}\right)^2}{2} = \frac{rc\ell^2}{4} + t_{buf}$$

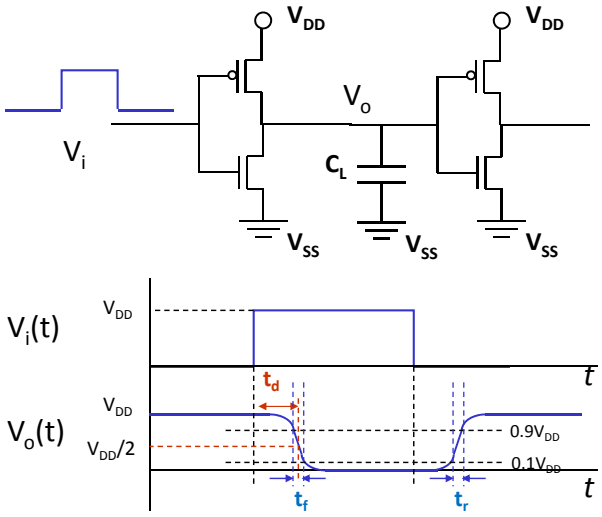
$t_{buf} << \frac{rc\ell^2}{4}$



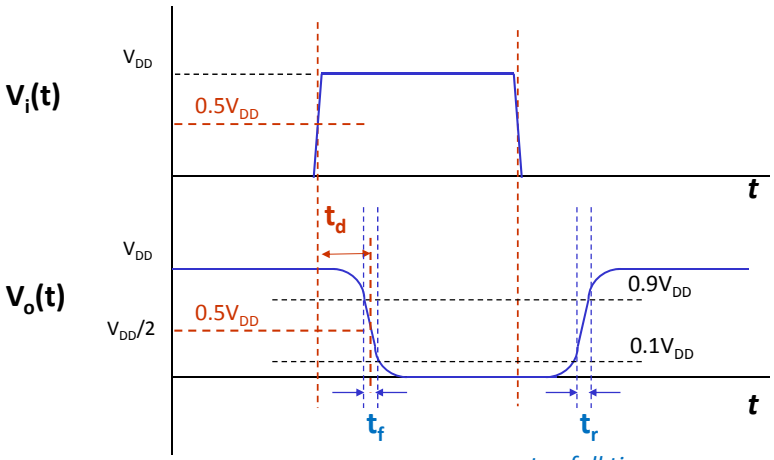
Equivalent Circuit

Gate Delay

Inverter Transition Characteristics



Transition Times



t_d = delay time

t_f = fall time
t_r = rise time

Fall and Rise Times

The fall time is given by the following equation:

$$t_f \approx d\frac{C_L}{k_n V_{DD}}$$

Similarly the rise time is:

$$t_r \approx d\frac{C_L}{k_p V_{DD}}$$

Given that the sizes of the nMOS and pMOS transistors are such that k_n=k_p then:

$$t_f = t_r$$

Propagation Delay Time – A

1st Approach

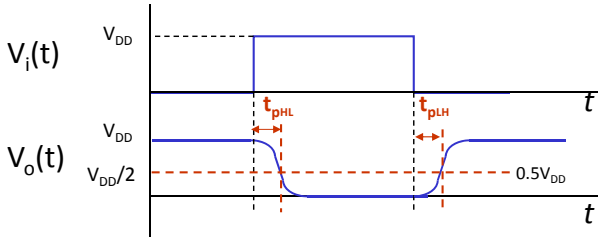
$$t_{pLH} \cong \frac{t_r}{2} \qquad t_{pHL} \cong \frac{t_f}{2}$$

Propagation delay:

$$t_p = \max(t_{pLH}, t_{pHL})$$

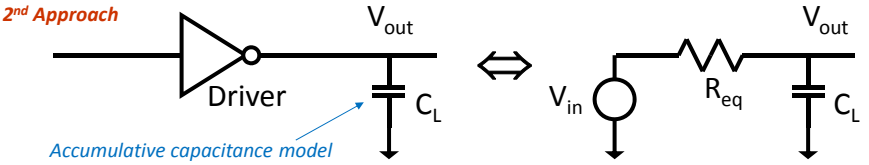
Average propagation delay:

$$t_{pav} = \frac{t_{pLH} + t_{pHL}}{2} = \frac{t_r + t_f}{4}$$



Propagation Delay Time – B

2nd Approach



The operation of the equivalent RC network is expressed by the following differential equation:

$$C_L \frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R_{eq}} = 0$$

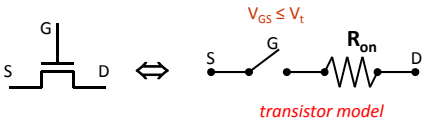
Applying a step input V_{in} (from 0 to V) it stands:

$$V_{out}(t) = (1 - e^{-t/\tau})V$$ *where $\tau = R_{eq} \times C_L$ is the time constant.*

For the rise of V_{out} to the 50% of V the time duration is: $t \equiv t_p = ln(2)\tau = 0.69\tau = 0.69\ R_{eq} \times C_L$ ✓

For the transition of V_{out} from 10% to 90% of V the time is: $t \equiv t_{r/f} = ln(9)\tau = 2.2\tau = 2.2 R_{eq} \times C_L$

The Transistor Model as Switch



Ron: { *time varying* / *nonlinear resistance* }

Approximation: we need to find a constant and linear equivalent resistance R_{eq} which will induce the same effect as the actual transistor. An initial estimation of R_{eq} can be the average value of the resistance R_{on} at the operating region under consideration.

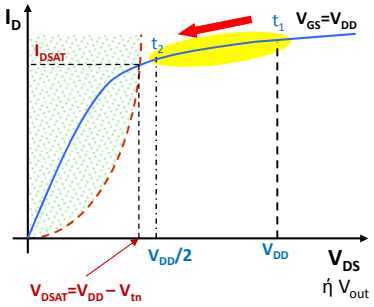
$$R_{eq} = \text{average}_{t=t_1..t_2}(R_{on}(t)) = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} R_{on}(t)dt \Rightarrow$$

$$R_{eq} = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)}dt \overset{?}{\cong} \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2))$$

(A) *(B)*

Transistor's Equivalent Resistance I

In order to determine the propagation delay time, the transistor's equivalent resistance during discharging (charging) of C_L, will be given by the following equation, considering that this time is defined as the time interval required in order V_{out} to change from V_{DD} (0) to $V_{DD}/2$ and during this time interval the transistor is in saturation ($V_{DD}>>V_{DSAT}$).



(A) $$R_{eq}=\frac{1}{t_2-t_1}\int_{t_1}^{t_2}\frac{V_{DS}(t)}{I_{DSAT}(1+\lambda V_{DS}(t))}dt=$$

$$=\frac{1}{-V_{DD}/2}\int_{V_{DD}}^{V_{DD}/2}\frac{V}{I_{DSAT}(1+\lambda V)}dV\cong$$

$$\cong\frac{3V_{DD}}{4I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

where: $$I_{DSAT}=k_n'\frac{W}{L}\left((V_{DD}-V_{tn})V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

$$k_n'=\frac{\mu_n\cdot\varepsilon}{t_{ox}}$$

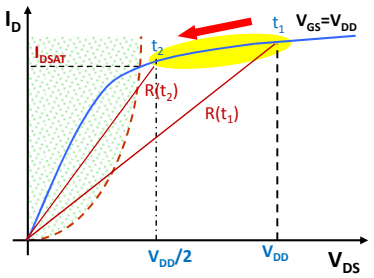
Transistor's Equivalent Resistance II

A similar equation is derived using the formula of the average resistance between the initial and the final state of the transistor.

(B) $$R_{eq}=\frac{1}{2}\left(R_{on}(t_1)+R_{on}(t_2)\right)=$$

$$=\frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})}+\frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right)\cong$$

$$\cong\frac{3V_{DD}}{4I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$



again: $$I_{DSAT}=k_n'\frac{W}{L}\left((V_{DD}-V_{tn})V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

$$k_n'=\frac{\mu_n\cdot\varepsilon}{t_{ox}}$$

Transistor's Equivalent Resistance III

$$R_{eq} = \frac{3V_{DD}}{4I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right) \cong \frac{3V_{DD}}{4I_{DSAT}} \Rightarrow$$

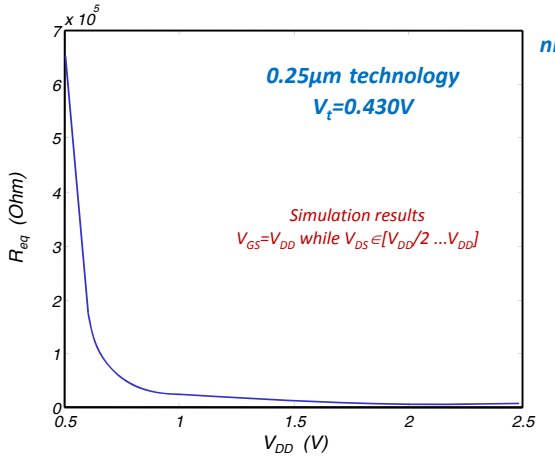
$$R_{eq} = \frac{3V_{DD}}{4k_n V_{DSAT}\left(V_{DD} - V_t - V_{DSAT}/2\right)} \Rightarrow$$

$$R_{eq} \cong \frac{3}{4}\frac{1}{k_n V_{DSAT}} = \frac{3}{4}\frac{1}{W/L\, k_n' V_{DSAT}} \Rightarrow \qquad k_n' = \frac{\mu_n \varepsilon}{t_{ox}}$$

$$R_{eq} \cong \frac{3}{4}\frac{L}{W}\frac{1}{k_n' V_{DSAT}}$$

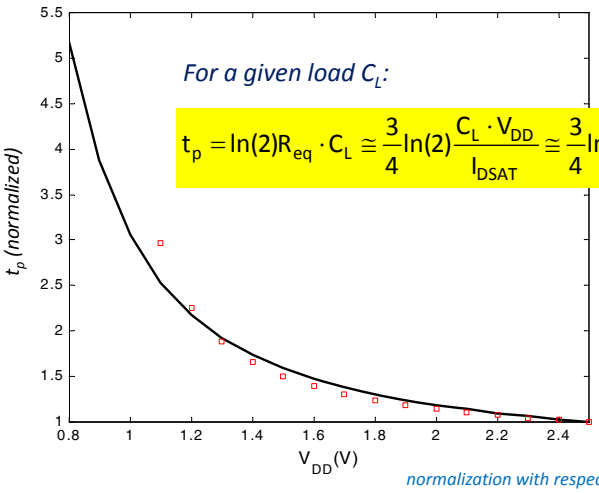
- *The equivalent resistance of a transistor is inversely proportional to W/L.*

Equivalent Resistance as a Function of V_{DD}



- *When $V_{DD} >> V_t + V_{DSAT}/2$ the resistance is independent of the power supply.*
- *When V_{DD} tend to the threshold voltage V_t the resistance rapidly increases.*

The Propagation Delay as a Function of V_{DD}

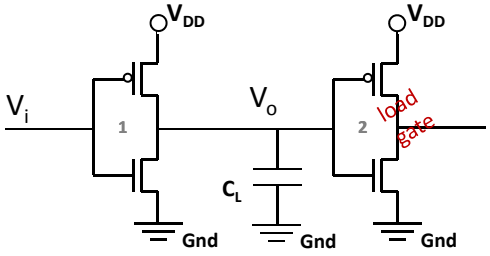


For a given load C_L:

$$t_p = \ln(2) R_{eq} \cdot C_L \cong \frac{3}{4}\ln(2)\frac{C_L \cdot V_{DD}}{I_{DSAT}} \cong \frac{3}{4}\ln(2)\frac{C_L}{k_n V_{DSAT}}$$

normalization with respect to the delay at 2.5V

Impact of k_p/k_n Ratio I



$$C_L = \underbrace{(C_{dp1}+C_{dn1})}_{C_{int}} + \underbrace{(C_{gp2}+C_{gn2})}_{C_{ext}} + C_w$$

In case that the size of pMOS is **β** times larger than this of nMOS, then all capacitances are scaled by the same factor:

$C_{dp1}=\beta C_{dn1}$ και $C_{gp2}=\beta C_{gn2}$

$$C_L = (1+\beta)(C_{dn1}+C_{gn2})+C_w$$

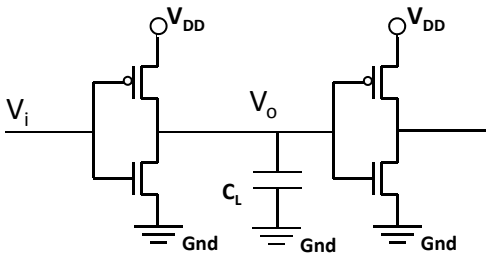
Average signal propagation delay of the 1st inverter :

$$t_{pav} = \frac{t_{pHL}+t_{pLH}}{2} = \frac{\ln(2)}{2}\left((1+\beta)(C_{dn1}+C_{gn2})+C_w\right)\cdot\left(R_{eqn}+\frac{R_{eqp}}{\beta}\right)$$

$$t_{pav} = 0.345\left((1+\beta)(C_{dn1}+C_{gn2})+C_w\right)\cdot R_{eqn}\left(1+\frac{r}{\beta}\right) \quad \textit{where: } r=\frac{R_{eqp}}{R_{eqn}},\ \beta=\frac{(W/L)_p}{(W/L)_n}$$

Note that R_{eqp} and R_{eqn} are the equivalent resistances of equal size pMOS and nMOS transistors respectivly

Impact of k_p/k_n Ratio II



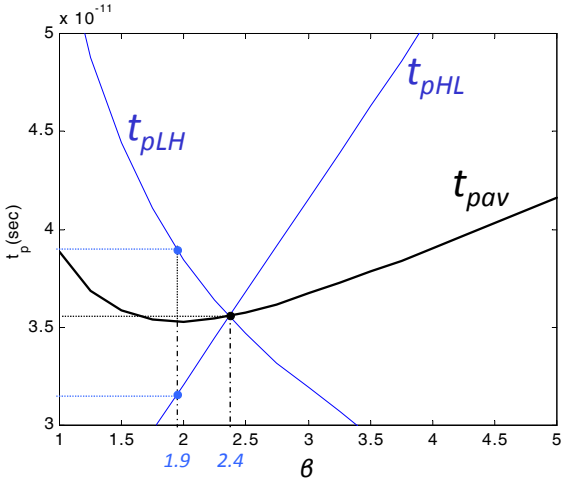
$$r = \frac{R_{eqp}}{R_{eqn}}$$

This ratio corresponds to pMOS and nMOS transistors of equal size.

The optimum value of β, with respect to time, is achieved by setting: $\frac{\partial t_{pav}}{\partial \beta} = 0$

$$\beta_{opt} = \sqrt{r\left(1 + \frac{C_w}{C_{dn1} + C_{gn2}}\right)}$$

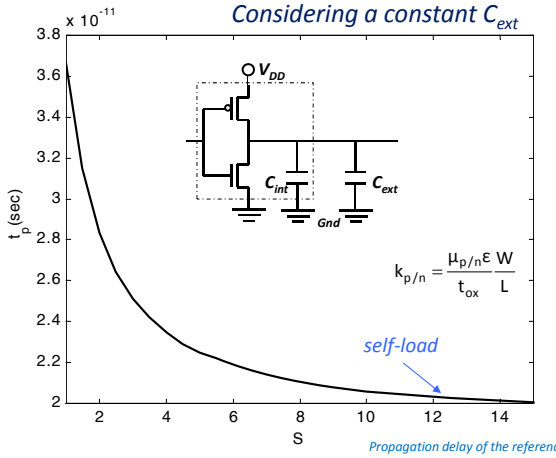
Impact of k_p/k_n Ratio III



$$\frac{k_p}{k_n} = \beta\frac{\mu_p}{\mu_n}$$

Reduced size transistors provide faster circuits at the expense of symmetry (reduced noise margins)!

Propagation Delay and Transistor Size



Considering a constant C_{ext}

Let us define as S the increment coefficient of the pMOS (k_p) and nMOS (k_n) transistor sizes in an inverter, with respect to a reference inverter which has the minimum size transistors.

$$k_{p/n} = S \cdot k_{p/n(ref)}$$

$$t_p = \ln(2) R_{eq} C_L = \ln(2) R_{eq} (C_{int} + C_{ext})$$

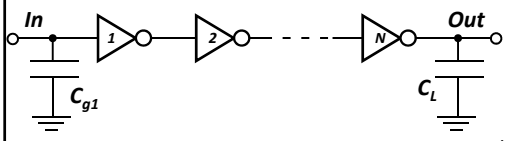
where:

$$R_{eq} = R_{ref}/S \qquad C_{int} = S \cdot C_{ref}$$

Propagation delay of the reference inverter without load (technology only dependence)

$$\Rightarrow \quad t_p = \ln(2) \frac{R_{ref}}{S} S \cdot C_{ref} \left(1 + \frac{C_{ext}}{S C_{ref}}\right) = \ln(2) R_{ref} \cdot C_{ref} \left(1 + \frac{C_{ext}}{S C_{ref}}\right) = t_{p0} \left(1 + \frac{C_{ext}}{S C_{ref}}\right)$$

Inverters' Sizes in a Chain (I)



Let us consider that: $C_{int} = \gamma C_g$ and $C_w = 0$

$\gamma \approx 1$ in modern technologies

$$t_p = t_{p0} \left(1 + \frac{C_{ext}}{C_{int}}\right) = t_{p0} \left(1 + \frac{C_{ext}}{\gamma C_g}\right) = t_{p0} \left(1 + f/\gamma\right)$$

$f = C_{ext}/C_g$

Consequently, at every stage of the inverters' chain it stands that:

$$t_{p,j} = t_{p0} \left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}}\right) = t_{p0} \left(1 + f_j/\gamma\right)$$

The total chain delay will be:

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{j=1}^{N} \left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}}\right) = t_{p0} \sum_{j=1}^{N} \left(1 + \frac{f_j}{\gamma}\right)$$

where: $C_{g,N+1} \equiv C_L$

Inverters' Sizes in a Chain (II)

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{j=1}^{N} \left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}} \right)$$

The equation has N–1 variables ($C_{g,j}$).

For the minimum delay we consider N–1 partial derivatives which are set equal to 0. Then, the following set of constrains will result:

$$\frac{\partial t_p}{\partial C_{g,j}} = 0$$

$$C_{g,j+1} / C_{g,j} = C_{g,j} / C_{g,j-1} \qquad j \in [2..N].$$

Consequently, the size of each inverter with respect to the previous one in the chain must increase by the same factor f, which means that f_j=f for every j. Given that $C_{g,1}$ and C_L are known, f is provided by the next equation:

$$f = \sqrt[N]{C_L / C_{g,1}} = \sqrt[N]{F} \qquad \textit{where:} \quad F = C_L / C_{g,1}$$

The minimum chain delay will be:

$$t_{pmin} = N \cdot t_{p0} \left(1 + \sqrt[N]{F} / \gamma \right)$$

The Optimum Number of Stages

$$t_{pmin} = N \cdot t_{p0} \left(1 + \sqrt[N]{F} / \gamma \right)$$

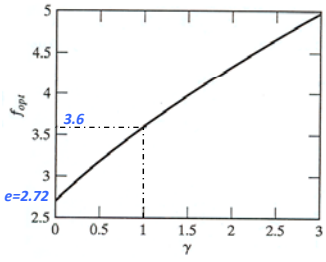
Which is the optimum number of stages?

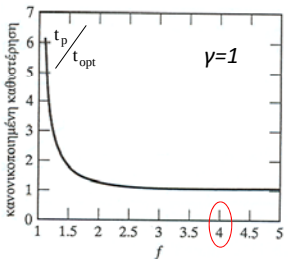
We consider the partial derivative with respect to N:

$$\frac{\partial t_{pmin}}{\partial N} = 0 \Rightarrow \gamma + \sqrt[N]{F} - \frac{\sqrt[N]{F} \cdot \ln(F)}{N} = 0$$

Neglecting self-load (γ=0) the optimum number of stages is : N = ln(F)

thus: $F = e^N$ and since: $f = \sqrt[N]{F} \Rightarrow$ f = e ≈ 2.7





Miller Effect

The Miller Effect (I)

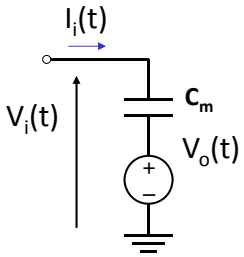
The voltage $V_o(t)$ is expressed by the equation:

$$V_o(t) = -AV_i(t-\tau) + V_o^*(t)$$

or equivalently for small τ<< (where τ is the delay):

$$V_o(t) = -A\left\{V_i(t) - \frac{dV_i(t)}{dt}\tau\right\} + V_o^*(t)$$

$V^*_o(t)$ is a component of V_o that is independent of V_i



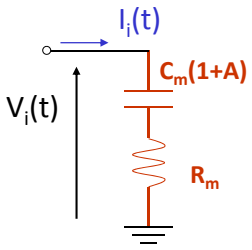
For the current $I_i(t)$ it stands:

$$I_i(t) = \frac{dq(t)}{dt} = C_m \frac{d}{dt}(\Delta V(t)) = C_m \frac{d}{dt}\left(V_i(t) - V_o(t)\right)$$

The Miller Effect (II)

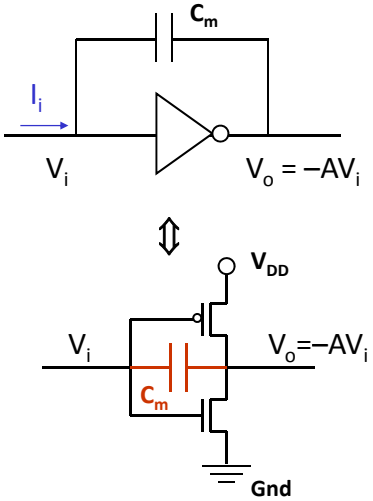
$$I_i(t) = C_m(1+A)\frac{d}{dt}\left\{V_i(t) - R_m C_m (1+A)\frac{dV_i(t)}{dt}\right\} - C_m \frac{dV_o^*(t)}{dt}$$

where: $R_m = \dfrac{A\tau}{C_m(1+A)^2}$

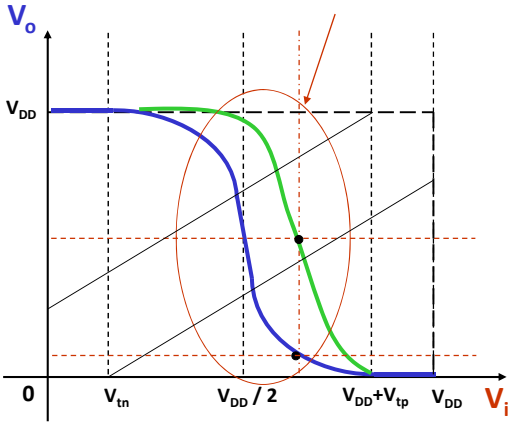


Consequently, for small τ << and neglecting the independent component $V^*_o(t)$, the next equivalent circuit is derived, where a capacitance $C_m(1+A)$ is in series with a resistance R_m.

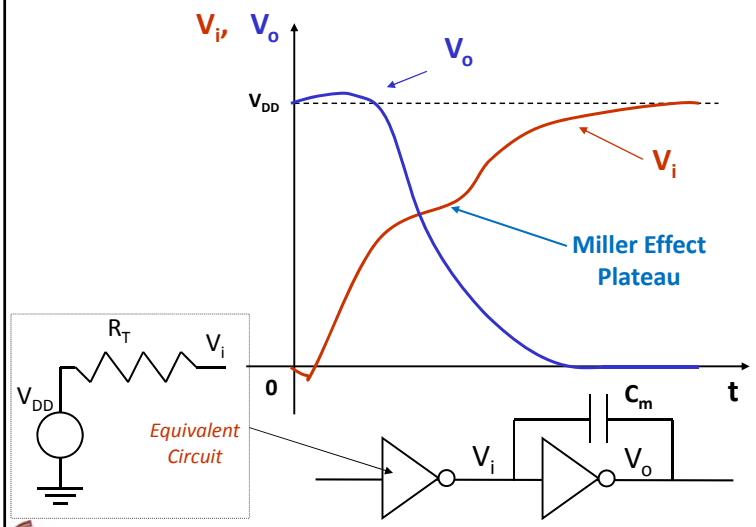
Miller Effect in CMOS Gates (I)



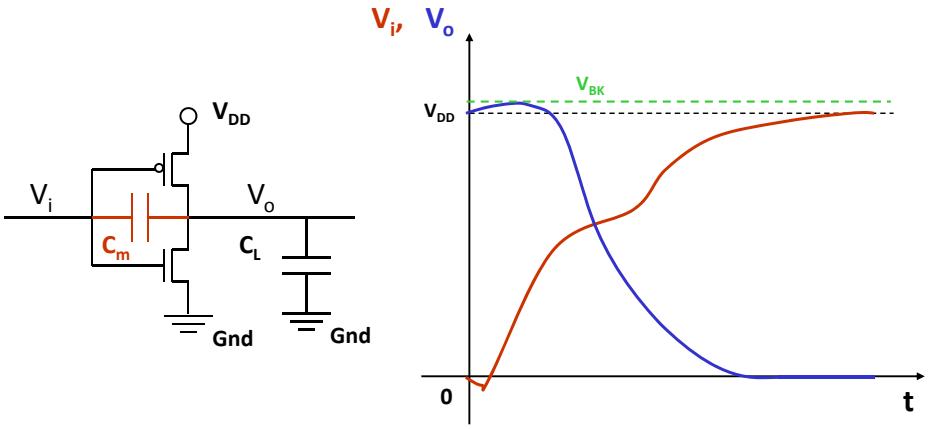
The apparent capacitance seen at the area of operation is $C_m(1+A)$.



Miller Effect in CMOS Gates (II)



Feed Forward I



Feed Forward II

Initially $V_i = 0$ and $V_o = V_{DD}$. Considering that the transition time of the input V_i from 0 to V_{DD} is short and that the nMOS transistor is very small, then according to the charge conservation law, the feed forward voltage V_{BK} can be estimated by the following equation :

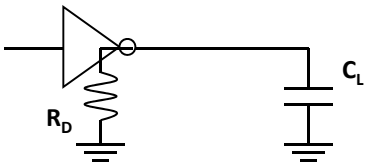
$$\underbrace{C_L V_{BK} + C_m (V_{BK} - V_{DD})}_{\text{finally}} = \underbrace{(C_m + C_L) V_{DD}}_{\text{initially}} \Rightarrow V_{BK} = V_{DD} + \frac{C_m}{C_L + C_m} V_{DD}$$

In the total duration of the output response we must include the time t_{BK} that is required by the nMOS transistor to discharge the output node back to V_{DD}:

$$t_{BK} = (C_L + C_m) \frac{V_{BK} - V_{DD}}{I_S}$$

Gate Transition Delay

The transition of a gate from a state (LOW/HI) to the complementary one (HI/LOW), is achieved by charging or discharging of the output load capacitance C_L through the MOS transistor resistance R_D.



The time delay constant is:

$$T_D = R_D \cdot C_L$$

Conventional approaches to reduce the transition delay consist in the design optimization by properly selecting the transistor sizes in order to reduce the parasitic resistances and capacitances.

Negative Resistance / Capacitance

The insertion of negative resistances or/and capacitances, according to the following schemes, may reduce the gate transition delay.

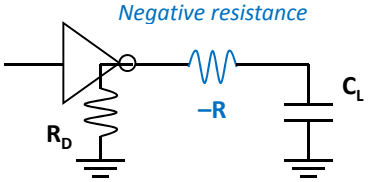
The time delay constant is :

$T'_D = (R_D - R) \cdot C_L = T_D - R \cdot C_L$

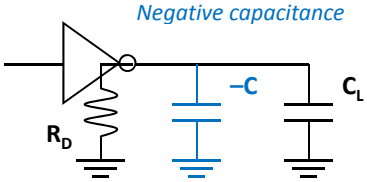
The time delay constant is :

$T''_D = R_D \cdot (C_L - C) = T_D - R_D \cdot C$

Negative resistance

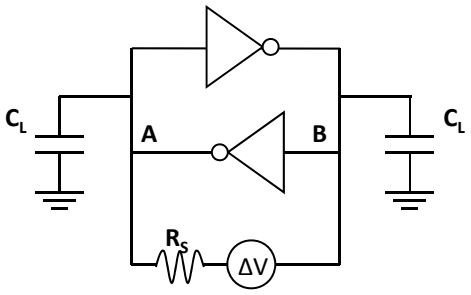


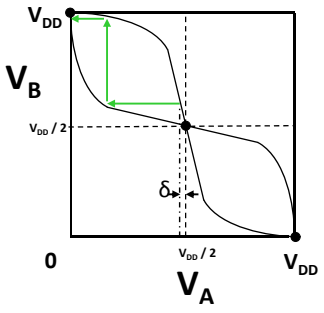
Negative capacitance



Negative Resistance

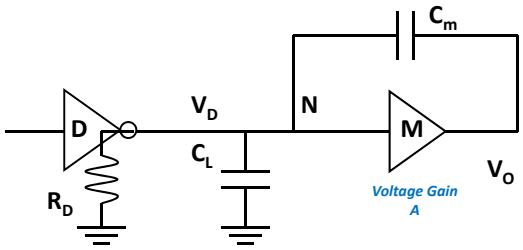
A possible way to insert a negative resistance is by the use of a differential amplifier, like the topology of a cross-coupled inverter pair. Given that the inverter pair is balanced (both inverters have the same transition threshold), an as small as difference ΔV in-between their inputs is rapidly amplified. This phenomenon is equivalent to the reduction of the internal resistance R_S of the source so that the virtual impedance at nodes A and B turns to be negative.





Negative Capacitance

A possible way to insert a negative capacitance is by exploiting the reverse Miller effect, e.g. by the use of a non-inverting amplifier M. Thus, during the transitions of gate D the capacitance at node N is reduced due to the Miller effect on M from C_L to C_L-(A-1)C_m.



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