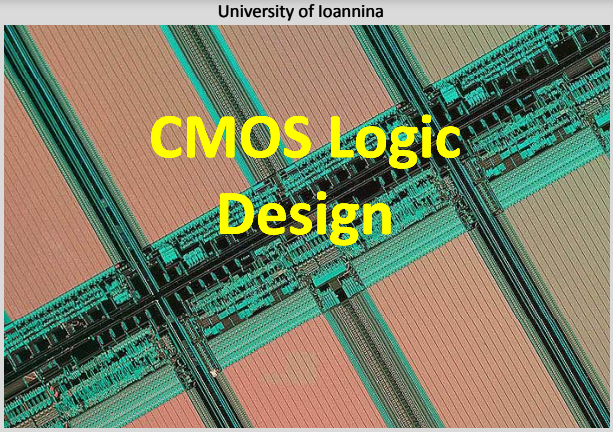
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

University of Ioannina



Dept. of Computer Science and Engineering

Survey on CMOS Digital Circuits

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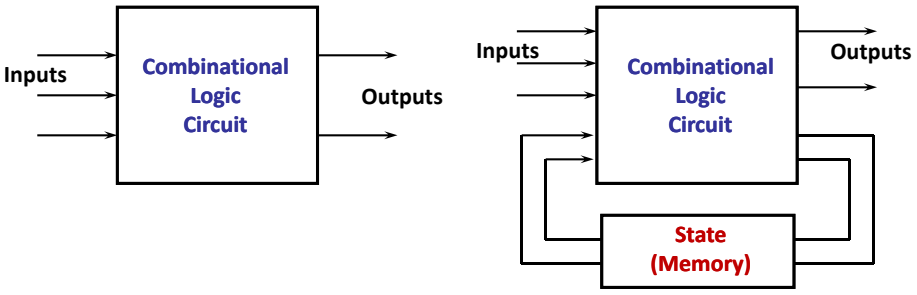
CMOS Integrated Circuit Design Techniques

Overview

1. Combinational – sequential logic
2. MOS transistor
3. CMOS logic
4. Complex gates
5. Standard cells

VLSI Systems
and Computer Architecture Lab

Combinational and Sequential Logic



Combinational Logic

outputs = f(inputs)

Sequential Logic

outputs= f(inputs, state)

Boolean Algebra

Axioms and Theorems

	$x + 0 = x$	$x \cdot 1 = x$
	$x + \bar{x} = 1$	$x \cdot \bar{x} = 0$
	$x + x = x$	$x \cdot x = x$
	$x + 1 = 1$	$x \cdot 0 = 0$
	$\bar{\bar{x}} = x$	
Permutation prop.:	$x + y = y + x$	$x \cdot y = y \cdot x$
Associative prop.:	$x + (y + z) = (x + y) + z$	$x \cdot (y \cdot z) = (x \cdot y) \cdot z$
Distributive prop.:	$x(y + z) = xy + xz$	$x + (y \cdot z) = (x + y) \cdot (x + z)$
De Morgan:	$\overline{x + y} = \bar{x} \cdot \bar{y}$	$\overline{x \cdot y} = \bar{x} + \bar{y}$
	$x + xy = x$	$x \cdot (x + y) = x$

Logic Gates

AND $F = x \cdot y$

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

OR $F = x + y$

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

NOT $F = \overline{x}$

x	F
0	1
1	0

BUFFER $F = x$

x	F
0	0
1	1

NAND $F = \overline{x \cdot y}$

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

NOR $F = \overline{x + y}$

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

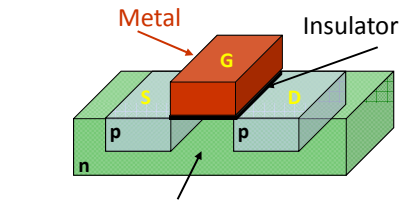
XOR $F = x \oplus y$

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

XNOR $F = \overline{x \oplus y}$

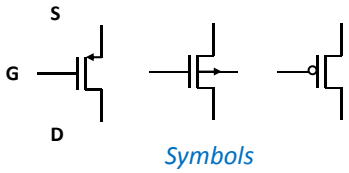
x	y	F
0	0	1
0	1	0
1	0	0
1	1	1

MOS Transistor

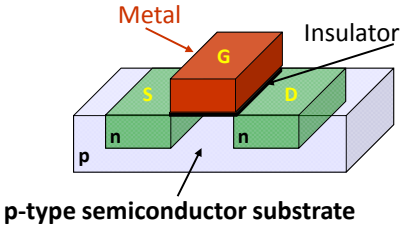


n-type semiconductor substrate

pMOS transistor

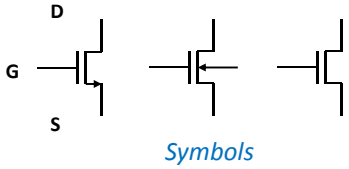


Symbols



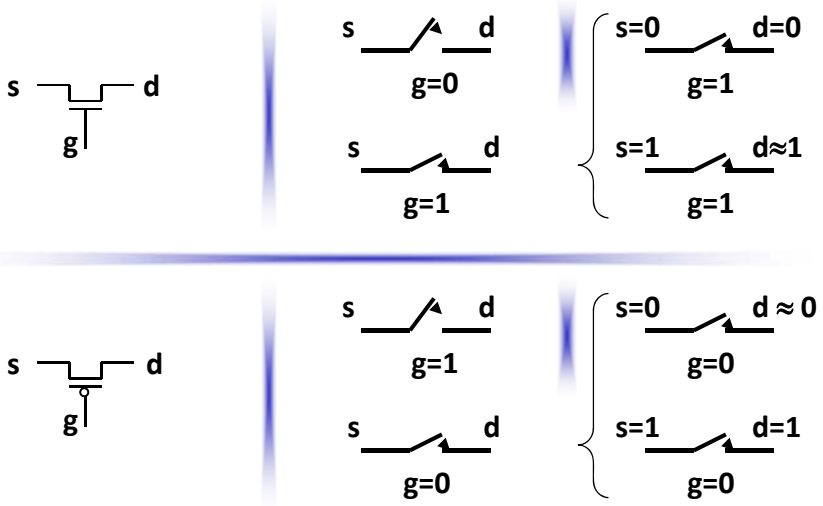
p-type semiconductor substrate

nMOS transistor

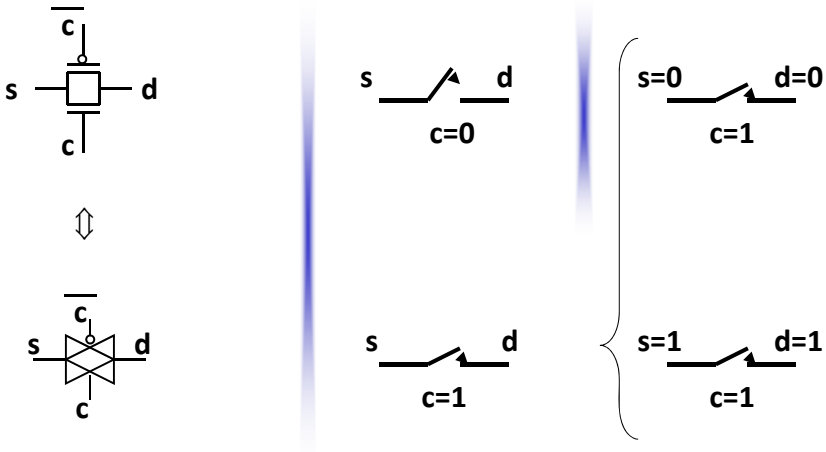


Symbols

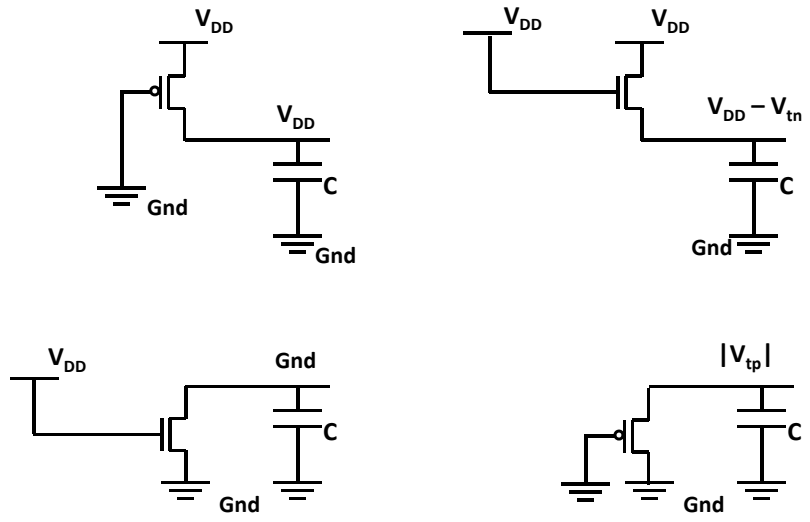
The MOS Transistor as Switch



The Full CMOS Switch

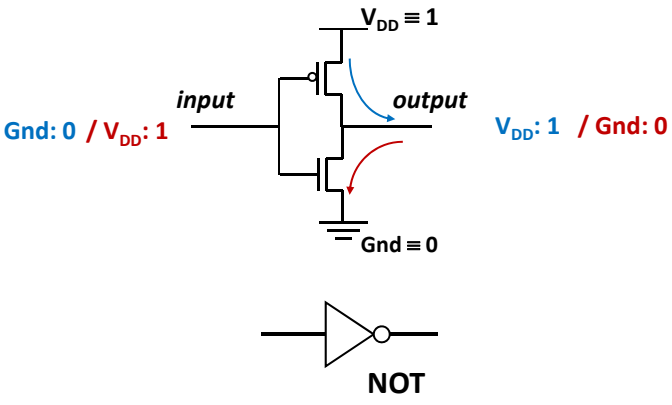


The Impact of Threshold Voltage

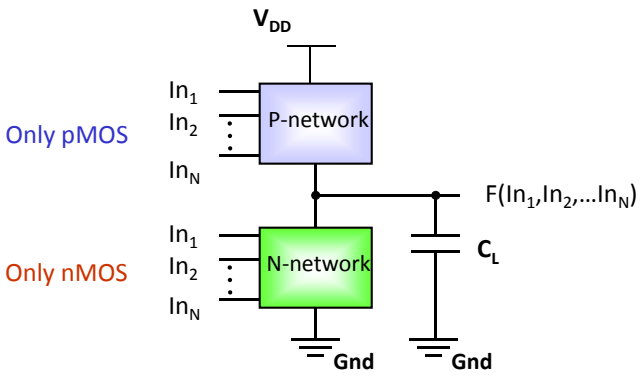


CMOS Logic

Inverter – NOT Gate



Static CMOS Gate



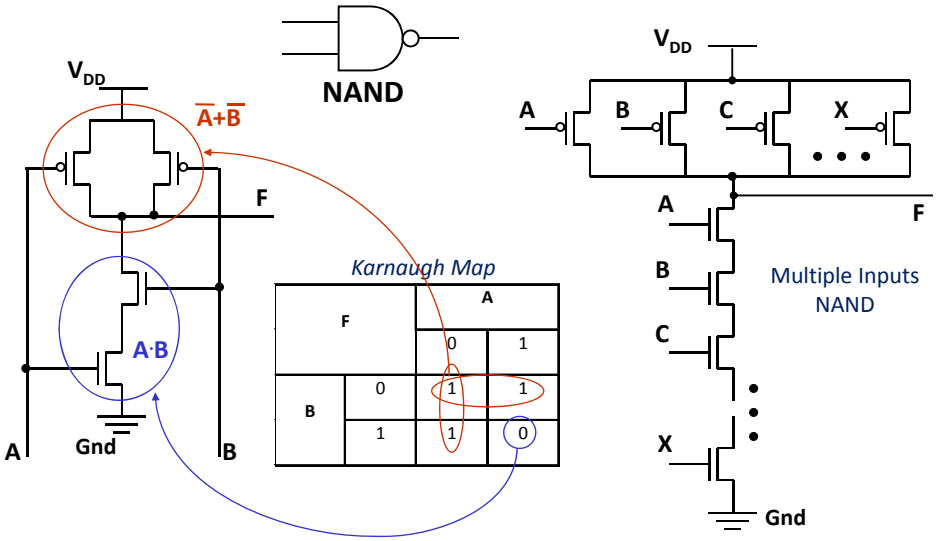
The P-network and N-network are ***complementary*** logic networks

Static CMOS Circuits

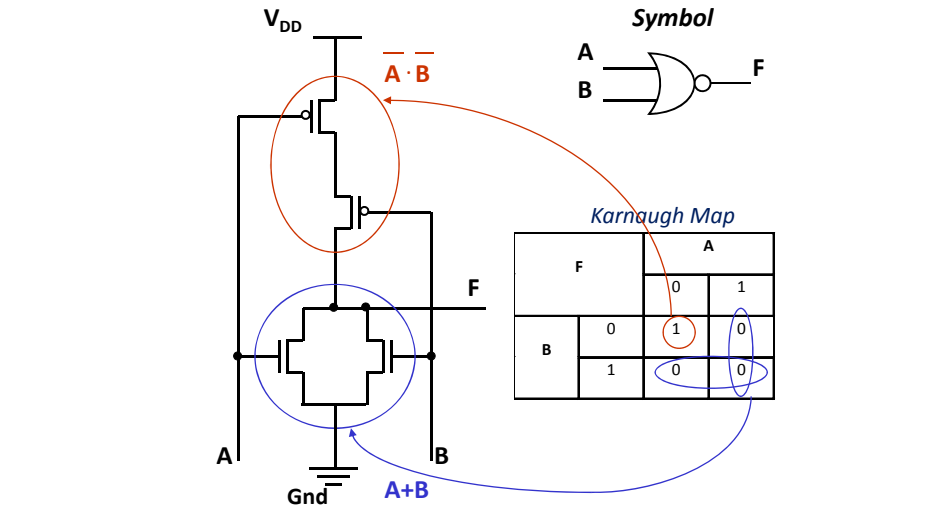
- Each time (except input transition intervals) the output of a static CMOS gate is always attached either to the V_{DD} power supply or the Gnd power supply. When a CMOS circuit is in the quiescent state, it is prohibitive for the two power supplies V_{DD} and Gnd to be connected (in a short circuit).

- The connection of the output to the V_{DD} power supply is through the pMOS network while the connection of the output to the Gnd power supply is through the nMOS network. When these networks are in a conducting state, behave as a low resistance resistor. In the opposite case, their resistance is considered to be infinite.

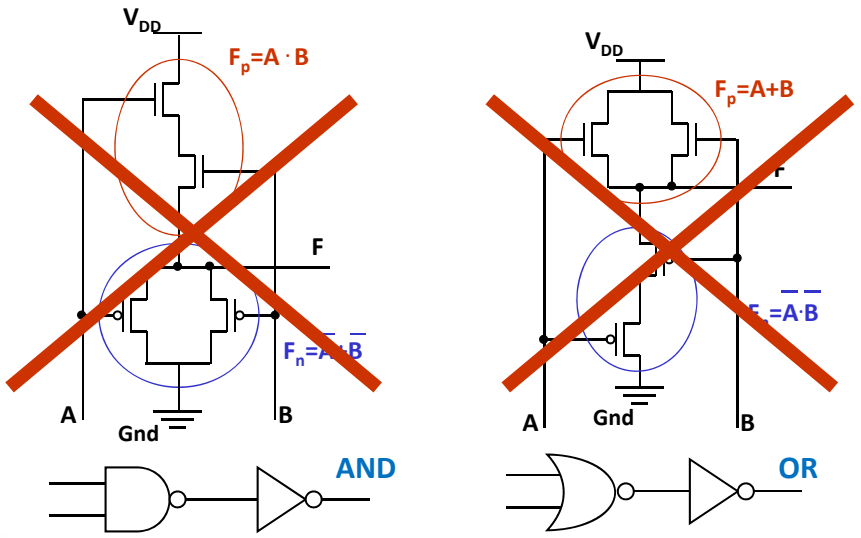
NAND Gate



NOR Gate



AND and OR Gates

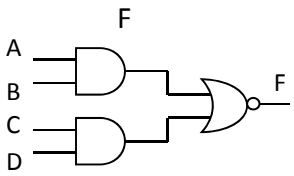


Complex Gates

Implementation of the function:

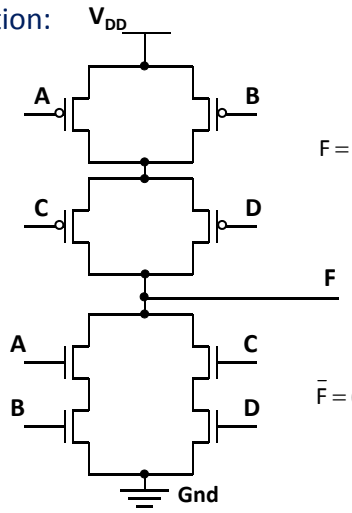
$$F=\overline{((A\cdot B)+(C\cdot D))}$$

pMOS network



nMOS network

$\overline{F}$

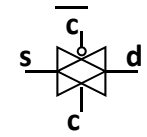


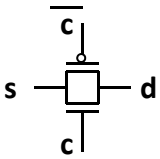
$$F=(\overline{A}+\overline{B})\cdot(\overline{C}+\overline{D})$$

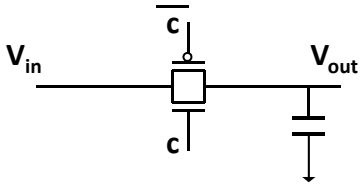
$$\overline{F}=((A\cdot B)+(C\cdot D))$$

CMOS Pass Gate

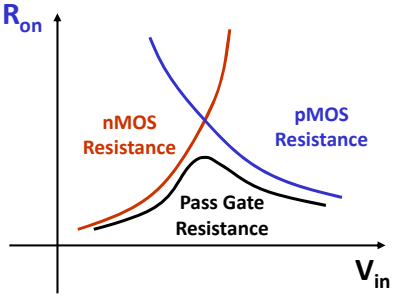
Symbols



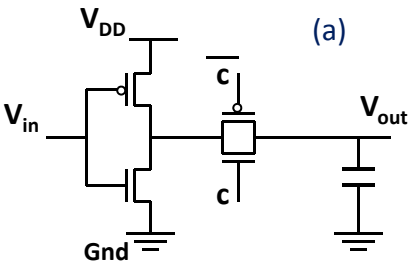


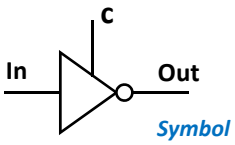


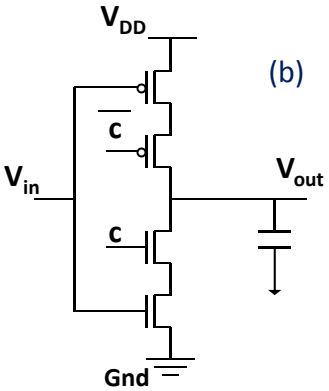
C = '0'	nMOS off pMOS off Vin='0', Vout= 'Z' Vin='1', Vout= 'Z'
C = '1'	nMOS on pMOS on Vin='0', Vout='0' Vin='1', Vout='1'



Tri-State Inverter



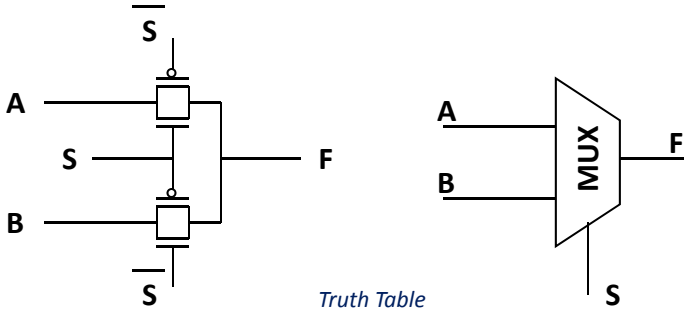




Truth Table

V_{in}	C	V_{out}
X	0	Z
0	1	1
1	1	0

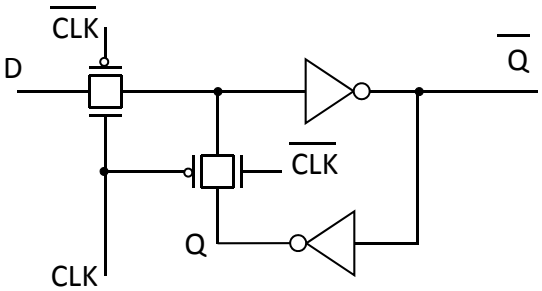
Multiplexer



Truth Table

A	B	S	F
X	0	0	0 (B)
X	1	0	1 (B)
0	X	1	0 (A)
1	X	1	1(A)

Latch



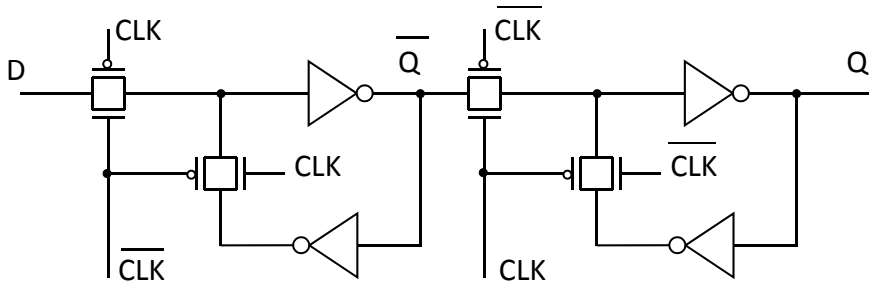
CMOS Latch

Truth Table

D	CLK	Q	Qbar
0	0	Memory	
0	1	0	1
1	0	Memory	
1	1	1	0

Memory Element

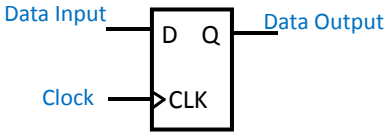
D Flip-Flop



CMOS Edge Triggered D Flip-Flop

D Flip-Flop Operation

Positive Edge-Triggered D Flip-Flop



Truth Table

D	CLK	Q	Qbar
X	0	Memory	
X	1	Memory	
0	0 → 1	0	1
1	0 → 1	1	0
X	1 → 0	Memory	