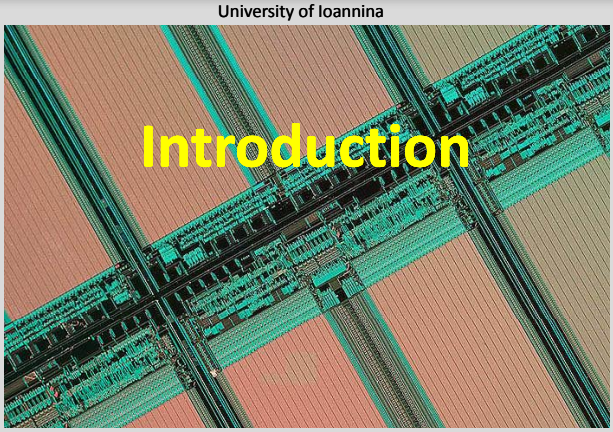
CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

University of Ioannina



Dept. of Computer Science and Engineering

Y. Tsiatouhas

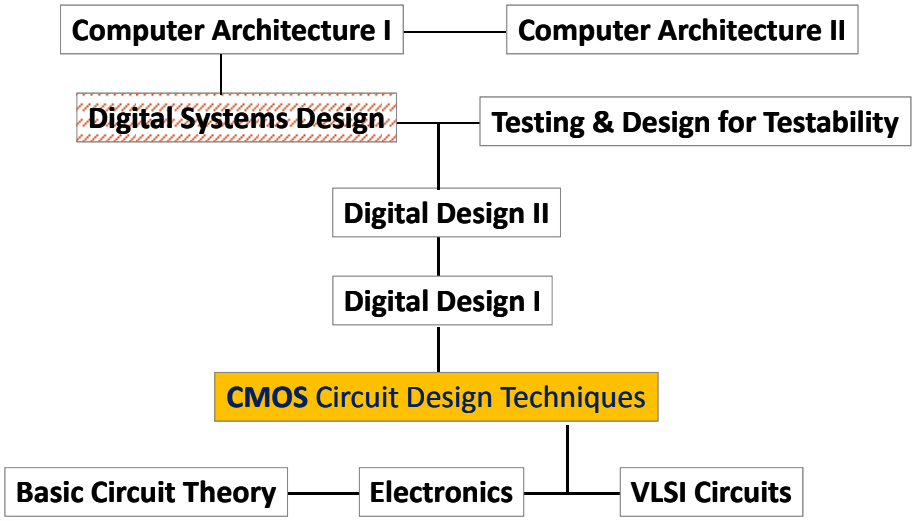
CMOS Integrated Circuit Design Techniques

VLSI Systems and Computer Architecture Lab

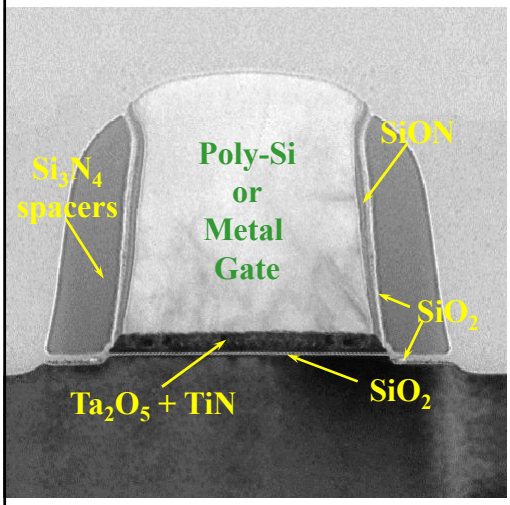
Course Objectives

- *CMOS integrated circuit design techniques*
  - *High performance design*
  - *Low-power – low-voltage design*
  - *Design for testability*

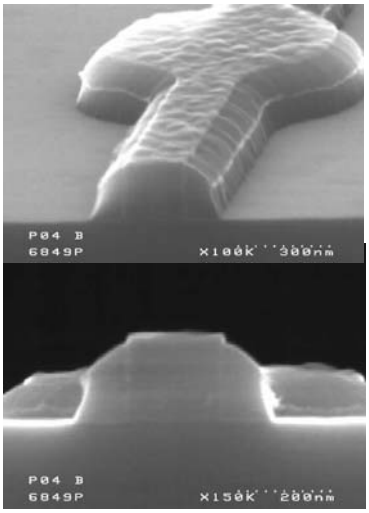
CSE Dept. – Courses on Electronics Design



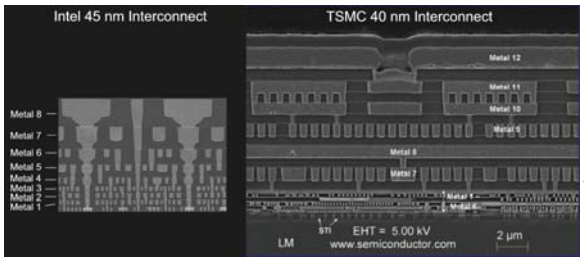
MOS Transistor

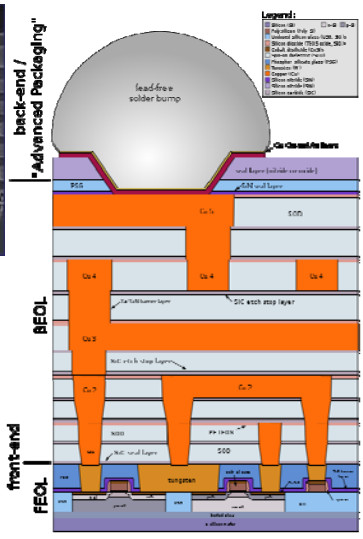


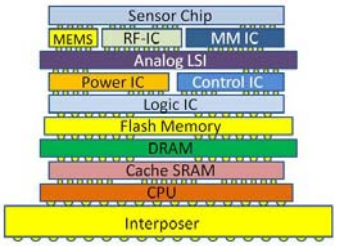
ST-Microelectronics



Integrated Circuits' Interconnects



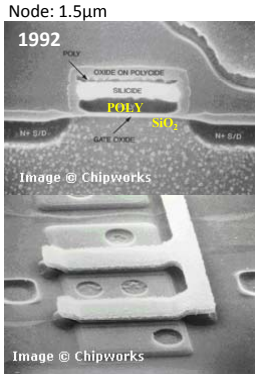




3D -Chips

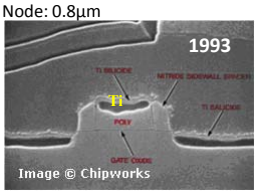
CMOS Technology Evolution (I)

Node: 1.5µm



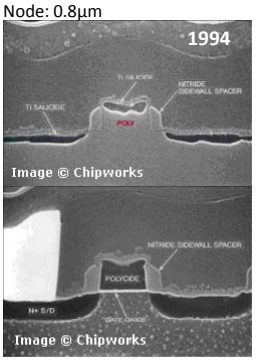
80386 – 16b – 16MHz, 1.1µm
BiCMOS
275K Xtors

Node: 0.8µm



Pentium, 0.65µm
BiCMOS
3.1M Xtors

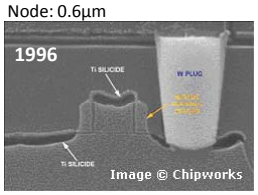
Node: 0.8µm



Pentium P54C, 0.45µm, 4m Al
BiCMOS

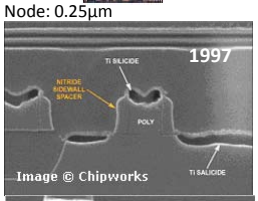
CMOS Technology Evolution (II)

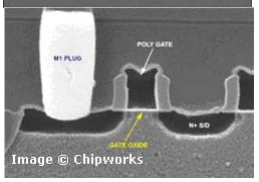
Node: 0.6µm



Pentium Pro – 200MHz, 0.35µm, 4m Al
BiCMOS
5.5M Xtors

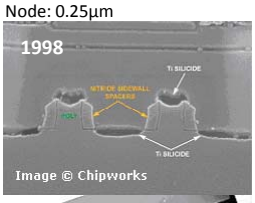
Node: 0.25µm

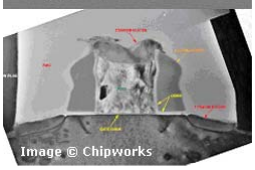




Pentium II – 32b – 266MHz, 0.25µm, 4m Al
CMOS
7.5M Xtors (Klamath)

Node: 0.25µm

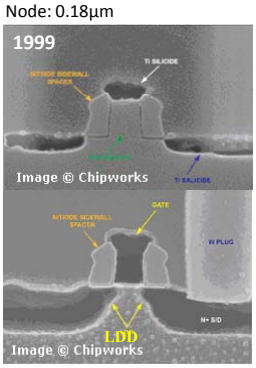




Pentium II –333MHz, 0.20µm, 5m Al
CMOS
(Deschutes)

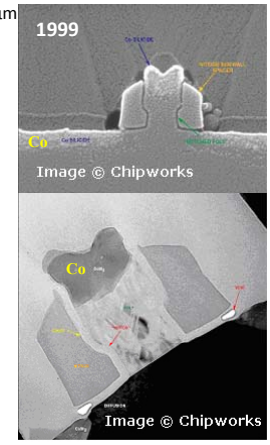
CMOS Technology Evolution (III)

Node: 0.18µm



Pentium III – 550MHz, 0.13µm, 5m Al CMOS
9.5M Xtors

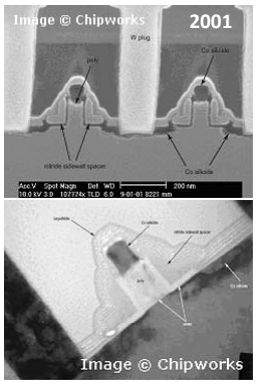
Node: 0.13µm



Pentium III – 650MHz, 0.08µm, 6m Al CMOS
(Coppermine)

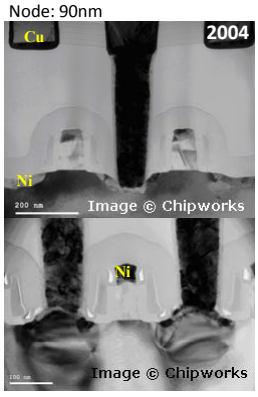
CMOS Technology Evolution (IV)

Node: 0.13µm



Pentium III – 1.2GHz, 0.07µm, 6m Cu CMOS
44M Xtors

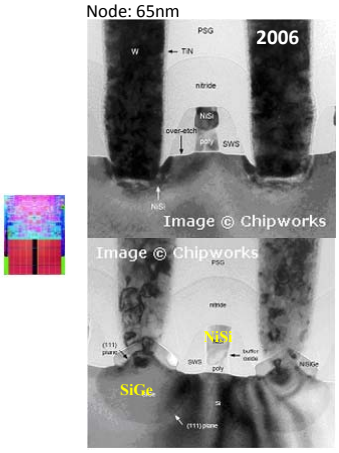
Node: 90nm



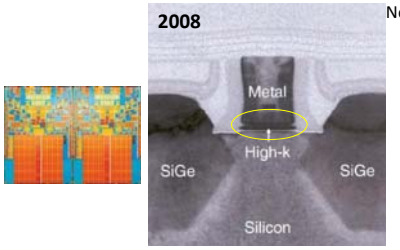
Pentium 4 – 2.8GHz, 0.045µm, 7m Cu CMOS
(Prescott)

CMOS Technology Evolution (V)

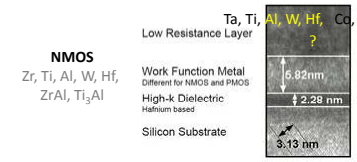
Node: 65nm



Dual Core D920 – 2.8GHz, 0.038µm, 8m Cu
CMOS
(Presler)



Node: 45nm



Ta, Ti, Al, W, Hf, Co, TiN
?

NMOS
Zr, Ti, Al, W, Hf, ZrAl, Ti_3Al
?

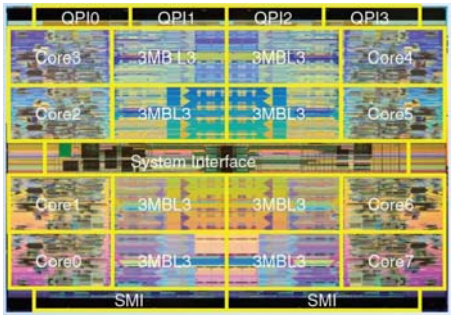
PMOS
Ru, Pa, Pt, Co, Ni, ZrAl, TiAlN
?

HfO_2 ή (HfSiO)
?

Core 2 Quad – 3GHz, 0.030µm, 9m Cu
CMOS
820M Xtors
(Penryn)

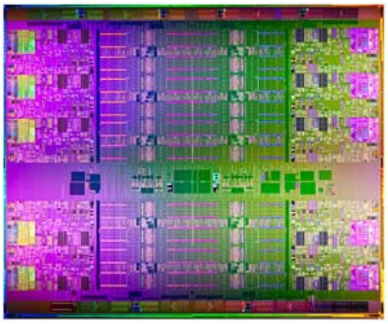
CMOS Technology Evolution (VI)

Node: 45nm 2009

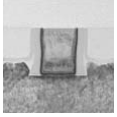


Xeon X7560 – 2.27 GHz
CMOS 45nm high K metal gate
2.3B Xtors
8 cores – 24MB L3
18 PLLs – 8 DLLs
Nehalem microarchitecture (Becton)
Cores: 0.85V – 1.1V, Cash: 0.9V
Clock gating + Power gating
Gate leakage: ↓25X nMOS, ↓1000 pMOS (w.r. 65nm)

Node: 32nm 2011

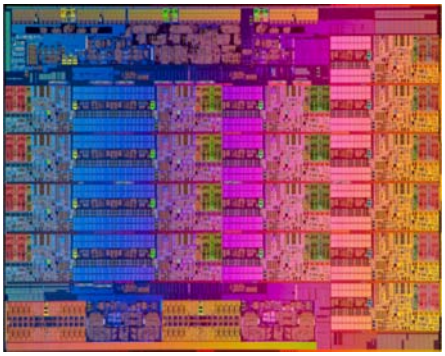


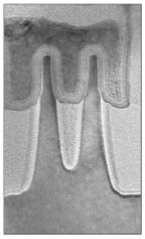
Xeon E7-8870 – 2.4 GHz
CMOS 32nm
10 cores – 30MB L3
Max memory size 4096 GB



CMOS Technology Evolution (VII)

Node: 14nm **2016**



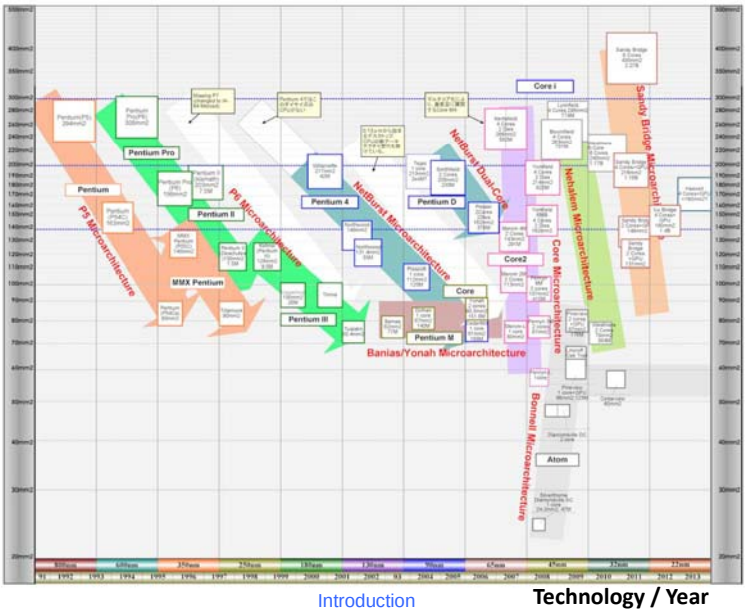


14 nm 2nd Generation
Tri-gate Transistor

Xeon E7-8890 v4 – 2.2-3.4 GHz
FinFET technology 14nm
24 cores – 60MB L3
Broadwell-EX (Brickland platform)
Max memory size 3.07 TB DDR4
Power 165W

Product Family	Intel Xeon E5-2600/4600 V4	Intel Xeon E7-8800/4800 V4	Intel Xeon E5-2600/4600 V5	Intel Xeon E7-8800/4800 V5	Intel Xeon E5-2600/4600 V6	Intel Xeon E7-8800/4800 V6
Family Branding	Broadwell-EP	Broadwell-EX	Skylake-EP	Skylake-EX	Cannonlake-EP	Cannonlake-EX
Process Node	14nm	14nm	14nm	14nm	10nm	10nm
Xeon Platform	Intel Grantley	Intel Brickland	Intel Purely	Intel Purely	Intel Purley	Intel Purley
PCH	C610 Series	C602J Series	Lewisburg PCH	Lewisburg PCH	Lewisburg PCH	Lewisburg PCH
Socket	Socket R3	Socket R1	Socket P	Socket P	Socket P	Socket P
Omni-Path (Interconnect)	N/A	N/A	Storm Lake Gen1	Storm Lake Gen1	Storm Lake Gen1	Storm Lake Gen1
Max Core Count	22	24	26	28	30-32?	32-34?
Max Thread Count	44	48	52	56	60-64?	64-68?
Max L3 Cache	55 MB	60 MB	65 MB	70 MB	75-80?	80-85?
Max PCI-Express Lanes	40 PCI-E Gen3	32 PCI-E Gen3	48 PCI-E Gen3	48 PCI-E Gen3	>48 PCI-E Gen3	>48 PCI-E Gen3
DDR4 Memory Support	4-Channel DDR4	4-Channel DDR4	6-Channel DDR4	6-Channel DDR4	6-Channel DDR4	6-Channel DDR4
TDP Range	55-145W	115-165W	45-160W	110-160W	45-160W	110-160W
Launch Expected	Q1 2016	Q2 2016	1H 2017	2017	2018	2018

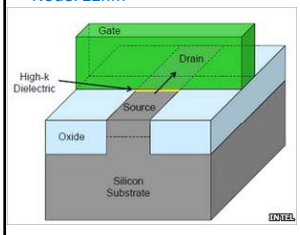
CMOS Technology Evolution (VI)

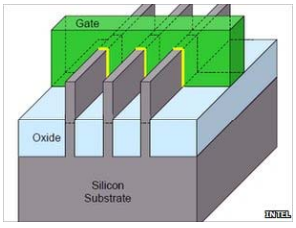


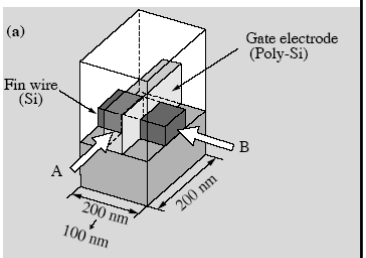
Intel

Nanometer Technologies Structures

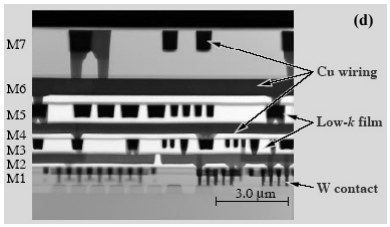
Node: 22nm



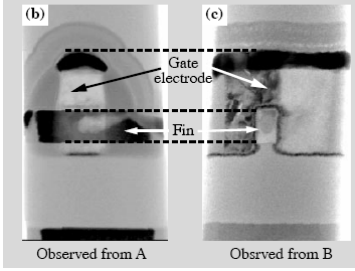




Fin-FET or 3D FET or Tri-Gate FET

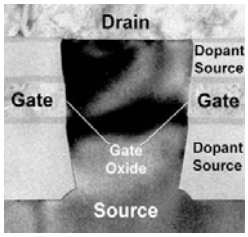


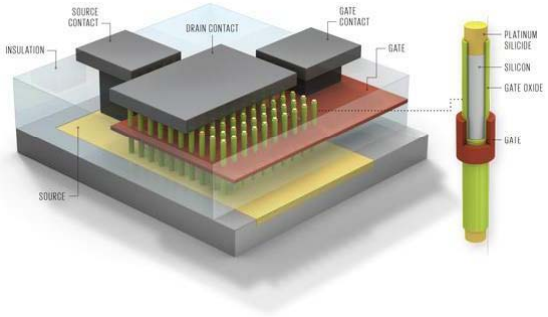
Hitachi

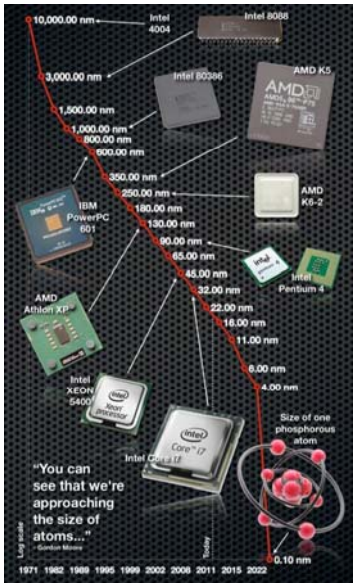


Nanometer Technologies Structures

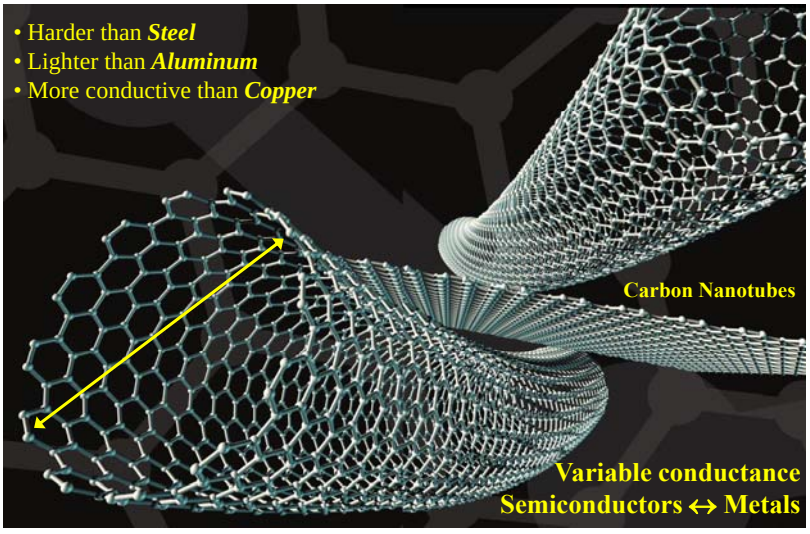
Vertical MOS





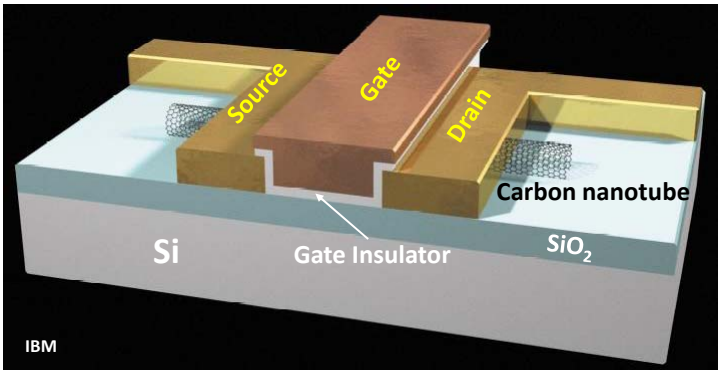


Carbon Nanotubes



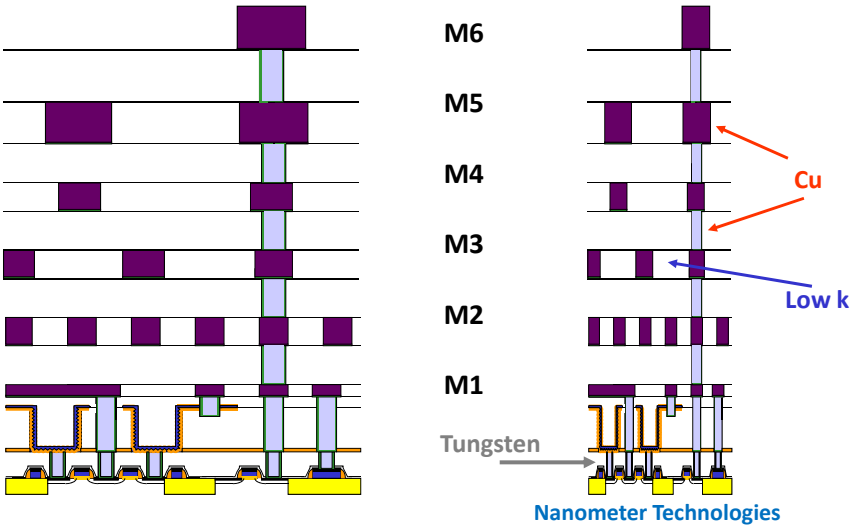
Carbon Nanotube FET

2nd generation

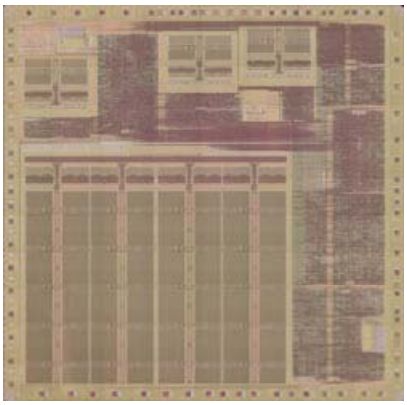


Development of ***p-type*** and ***n-type*** FETs

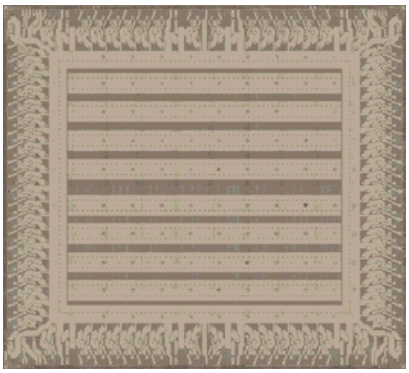
CMOS Technology Scaling



Very Large Scale Integration – VLSI

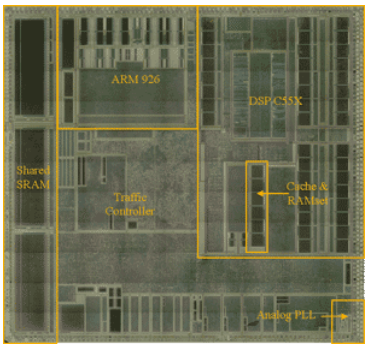


ASIC

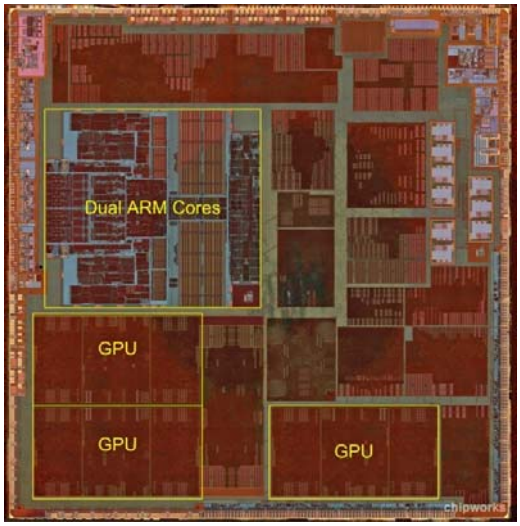


FPGA

Systems-on-Chip

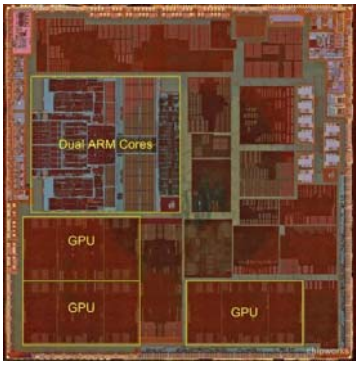


Texas Instruments

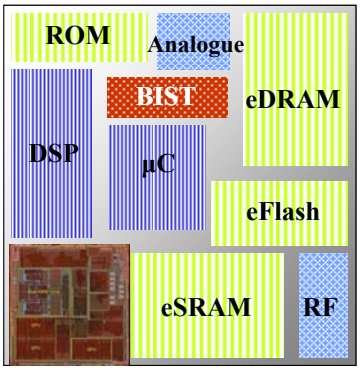


System-on-a-Chip (SoC)

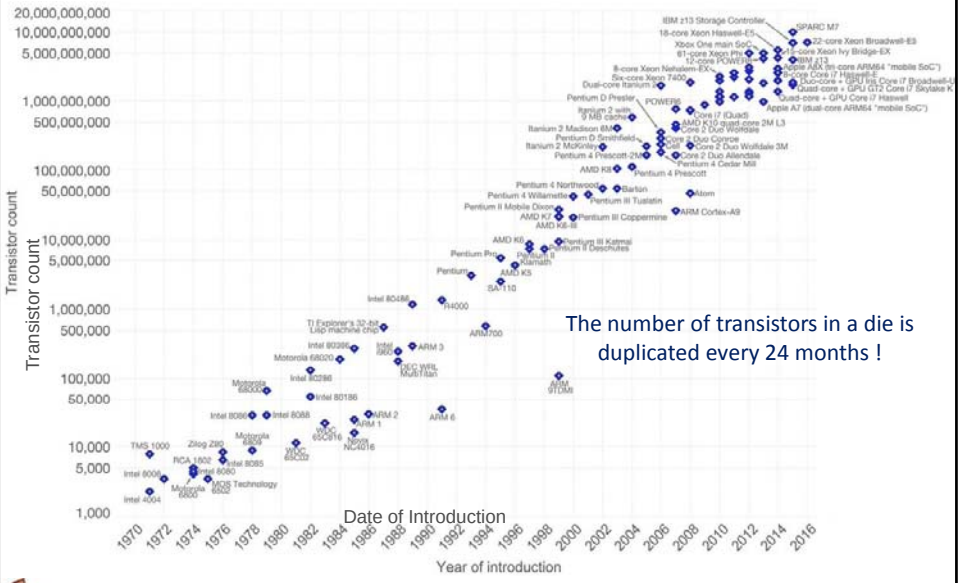
65nm CMOS



22nm CMOS



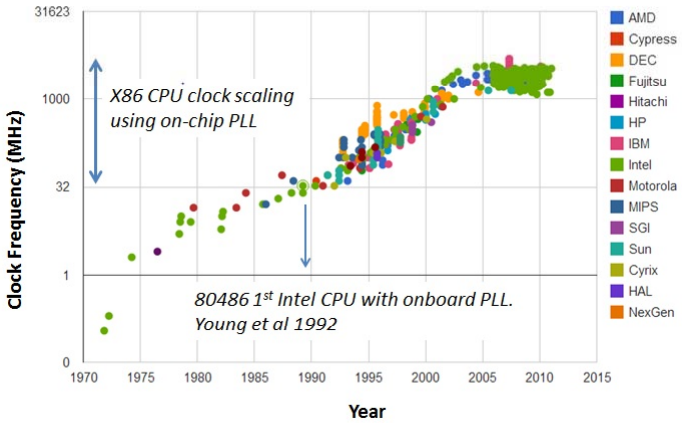
The Moore's Law



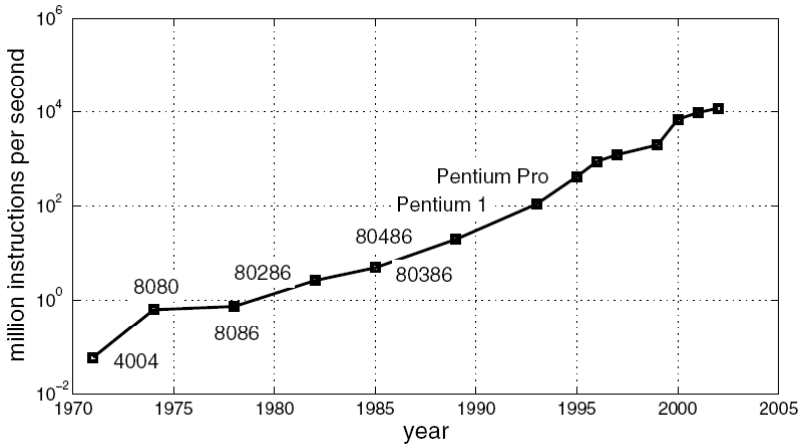
The number of transistors in a die is duplicated every 24 months !

Date of Introduction

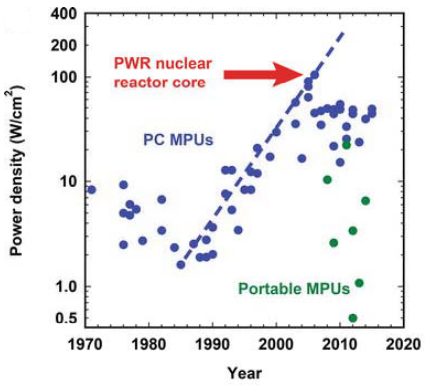
Frequency

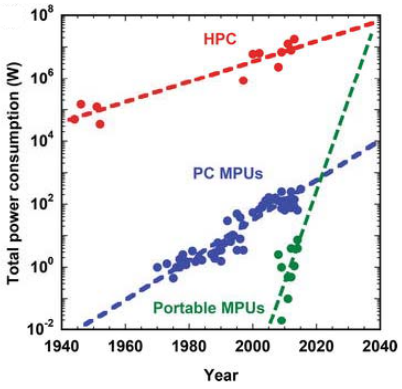


Performance



Power Consumption/Density

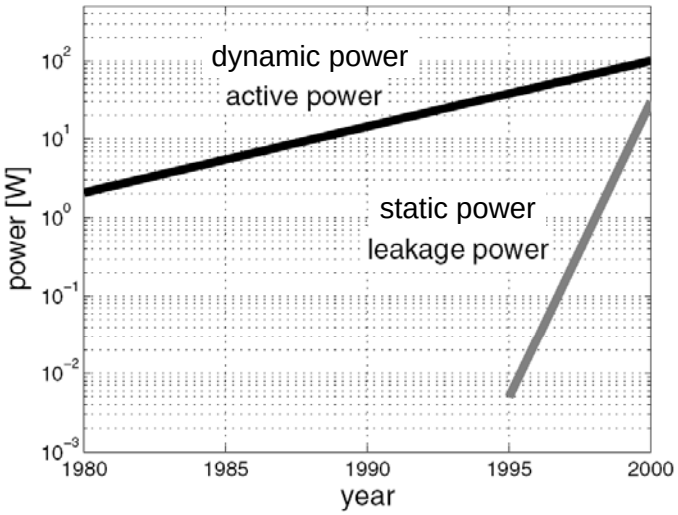




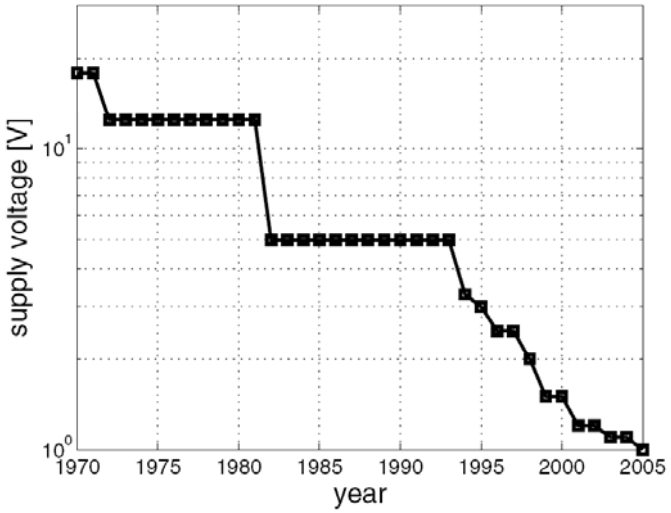
Dark Silicon !

ICT - Energy Concepts for Energy Efficiency and Sustainability, Fagas, et al, 2017

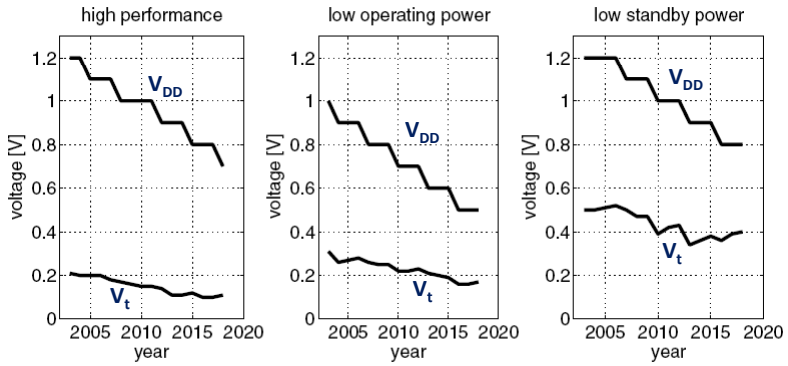
Dynamic & Static Power Consumption



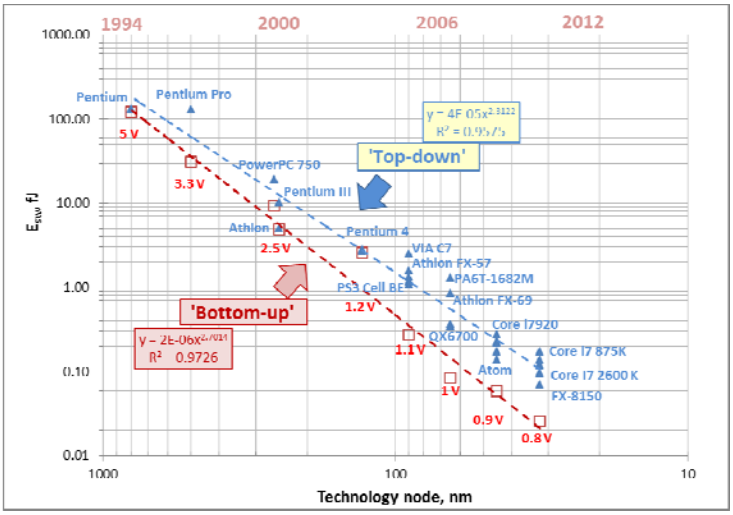
Power Supply Scaling



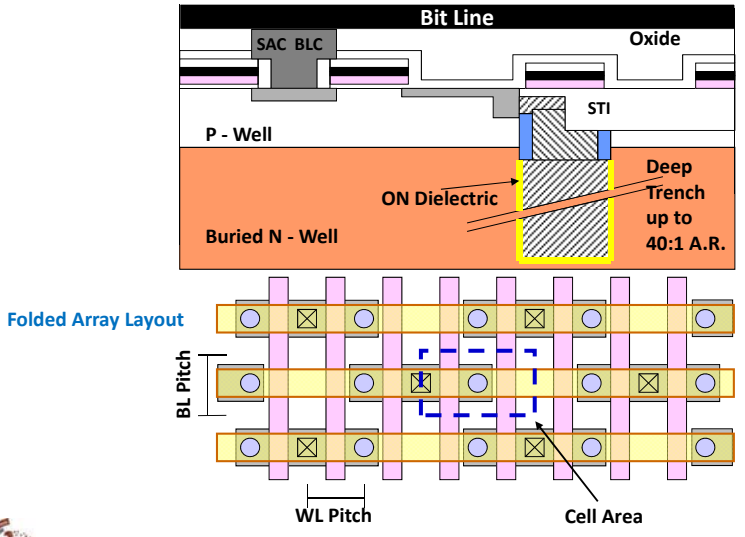
Power Supply (V_{DD}) & Threshold Voltage (V_t)



Transistor's Switch Energy



Design-Manufacturing Constraints



Transistor and trench capacitor aspect ratio in 180 nm technology

Process Variations (I)

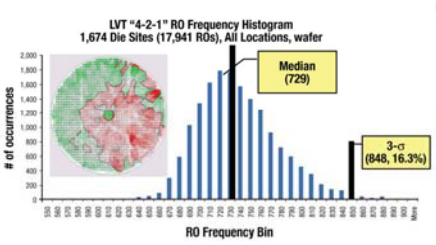
Transistor (and in general device) manufacturing parameters are varying from wafer to wafer and from die to die. These variations are called process variations, they are random and not correlated and they are due to:

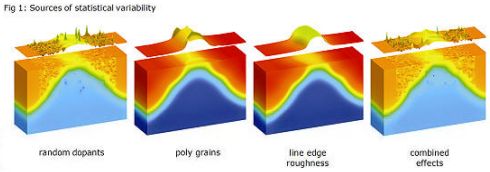
- *variations in the oxide thickness, in the depth of the diffusion area, in the dopant concentration e.t.c.*
- *geometric variations, like the transistor W/L ratio or the width of the interconnect metal lines.*

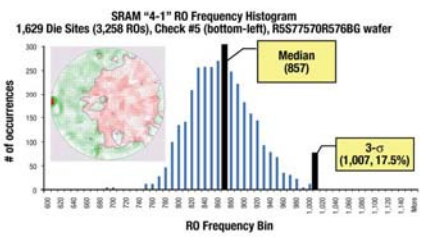
Process variations result in positive or negative deviations from the expected circuit operation. Aiming to support the design phase, semiconductor companies provide "fast" and "slow" device models that correspond to ± 3σ parameter deviations with respect to the nominal values, as well as statistical models in order to be able to predict the circuit response through simulations or Monte-Carlo analysis respectively.

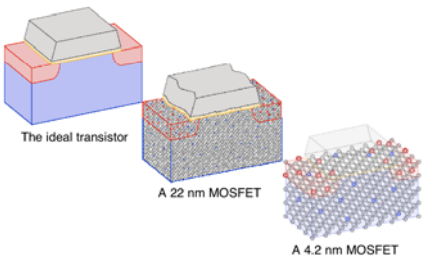
Process variations tend to increase with technology evolution!

Process Variations (II)



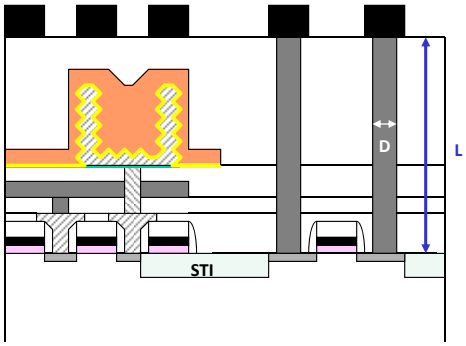




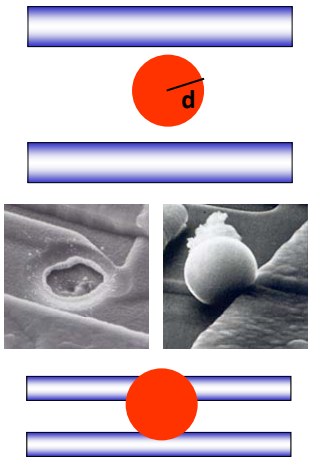


Manufacturing Defects

Contact aspect ratio: L/D = 7/1
0.18µm Technology

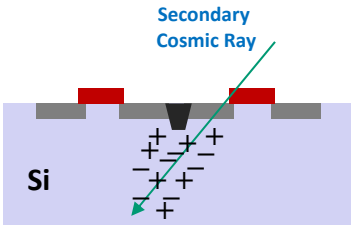


d = defect size

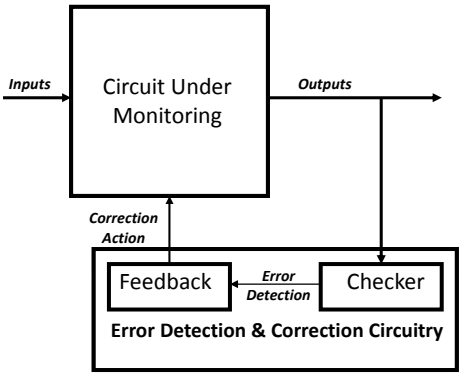


Nanometer Technologies

Transient Faults



Burst of Electronic Charge
1M electrons/µm Si



ITRS – High Performance (I)

Process Integration - Devices

Year
Technology node
Physical gate length (high perform.)
EOT: Equiv. oxide thickness
Max. gate leakage current density
V_{DD}: power supply
V_{tsat}: Saturation threshold voltage
I_{off}: S/D subthreshold leakage current
I_{Dsat}: NMOS drive current
Mobility enhancement factor

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
L_g Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	12	11	11	10	8	6.5	6	6	
UTB FD (Å)				8	8	7	6	5	5
DG (Å)							5	5	5
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]									
Extended Planar Bulk (Å)	19.3	18.4	18.4	17.0	16.0	9.2	7.5	7.5	
UTB FD (Å)				11	11	11	10	9	9
DG (Å)							12	11	10
$J_{g\,max}$ Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm²)	1.88E+02	5.36E+02	8.00E+02	1.18E+03	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
UTB FD (A/cm²)				7.73E+02	9.50E+02	1.22E+03	1.38E+03	2.07E+03	2.23E+03
DG (A/cm²)							6.25E+02	7.86E+02	8.46E+02
V_{dd} Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
$V_{t,sat}$ Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	195	168	165	164	237	151	146	148	
UTB FD (mV)				168	168	167	170	166	167
DG (mV)							181	184	186
$I_{off\,max}$ Source-Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (µA/µm)	0.06	0.15	0.2	0.28	0.22	0.28	0.32	0.34	
UTB FD (µA/µm)				0.32	0.40	0.22	0.22	0.29	0.29
DG (µA/µm)							0.1	0.11	0.11
$I_{d,sat}$ effective NMOS Drive Current [9]									
Extended Planar Bulk (µA/µm)	1.02E+03	1.13E+03	1.26E+03	1.21E+03	1.18E+03	2.05E+03	2.49E+03	2.30E+03	
UTB FD (µA/µm)				1400	1640	1815	2015	2037	2198
DG (µA/µm)							1899	1932	2220
Mobility Enhancement Factor for $I_{d,sat}$ [10]									
Extended Planar Bulk	1.09	1.09	1.08	1.09	1.1	1.1	1.12	1.11	
UTB FD				1.08	1.08	1.08	1.06	1.05	1.05
DG							1.05	1.04	1.05

ITRS

International Technology Roadmap for Semiconductors

ITRS – High Performance (II)

Process Integration - Devices

Year
Technology node
Physical gate length (high perform.)
EOT: Equiv. oxide thickness
Max. gate leakage current density
V_{DD}: power supply
V_{tsat}: Saturation threshold voltage
I_{off}: S/D subthreshold leakage current
I_{Dsat}: NMOS drive current

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
L_g Physical L_{gate} for High Performance logic (nm) [1]	11	10	9	8	7	6	5
EOT: Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	5	5					
DG (Å)	6	6	5	5	5	5	5
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]							
Extended Planar Bulk (Å)							
UTB FD (Å)	9	9					
DG (Å)	10	10	9	9	9	9	9
$J_{g\,max}$ Maximum gate leakage current density [5]							
Extended Planar Bulk (A/cm²)							
FDSOI (A/cm²)	3.27E+03	3.70E+03					
DG (A/cm²)	1.00E+03	1.10E+03	1.22E+03	1.38E+03	1.57E+03	1.83E+03	2.20E+03
V_{dd} Power Supply Voltage (V) [6]	0.9	0.8	0.8	0.7	0.7	0.7	0.7
$V_{t,sat}$ Saturation Threshold Voltage [7]							
Extended Planar Bulk (mV)							
UTB FD (mV)	164	166					
DG (mV)	190	192	195	200	201	205	208
$I_{off\,max}$ Source-Drain Subthreshold Off-State Leakage Current [8]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	0.36	0.37					
DG (µA/µm)	0.11	0.11	0.11	0.11	0.11	0.11	0.11
$I_{d,sat}$ effective NMOS Drive Current [9]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	2290	2188					
DG (µA/µm)	2354	2275	2713	2533	2740	2744	2981

ITRS – Low Leakage (I)

Process Integration - Devices

	Year in Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
Year	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
Technology node	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
Physical gate length (low static power)	L_g: Physical gate length for LSTP [1]									
	Extended Planar Bulk and DG (nm)	65	53	45	37	32	28	25	22	20
	UTB FD (nm)								22	20
EOT: Equiv. oxide thickness	EOT: Equivalent Oxide Thickness [2]									
	Extended planar bulk (Å)	21	20	19	16	15	14	14	13	12
	UTB FD (Å)								12	11
	DG (Å)								13	12
V_{DD}: power supply	V_{dd}: Power Supply Voltage (V) [6]	1.2	1.2	1.2	1.1	1.1	1.1	1	1	1
V_{tsat}: Saturation threshold voltage	$V_{t,sat}$: Saturation Threshold Voltage [7]									
	Extended Planar Bulk (mV)	482	515	524	501	501	502	502	491	483
	UTB FD (mV)								483	486
	DG (mV)								441	435
I_{off}: S/D subthreshold leakage current	$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
	Extended Planar Bulk (µA/µm)	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.2E-05	1.6E-05	2.1E-05
	UTB FD (µA/µm)								1.0E-05	1.0E-05
	DG (µA/µm)								1.0E-05	1.0E-05
I_{Dsat}: NMOS drive current	$I_{d,sat}$: effective NMOS Drive Current [9]									
	Extended Planar Bulk (µA/µm)	497	500	519	573	612	666	580	625	684
	UTB FD (µA/µm)								678	719
	DG (µA/µm)								673	747

ITRS – Low Leakage (II)

Process Integration - Devices

	Year in Production	2014	2015	2016	2017	2018	2019	2020
Year	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
Technology node	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
Physical gate length (low static power)	L_g: Physical gate length for LSTP [1]							
	Extended Planar Bulk and DG (nm)	18	16	14	13	12	11	10
	UTB FD (nm)	18	17	16	15	14	13	12
EOT: Equiv. oxide thickness	EOT: Equivalent Oxide Thickness [2]							
	Extended planar bulk (Å)							
	UTB FD (Å)	10	9	8	8	8	8	8
	DG (Å)	11	11	11	10	10	9	9
V_{DD}: power supply	V_{dd}: Power Supply Voltage (V) [6]	1	1	1	1	1	1	1
V_{tsat}: Saturation threshold voltage	$V_{t,sat}$: Saturation Threshold Voltage [7]							
	Extended Planar Bulk (mV)							
	UTB FD (mV)	486	489	487	487	492	488	486
	DG (mV)	432	434	436	438	440	443	443
I_{off}: S/D subthreshold leakage current	$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]							
	Extended Planar Bulk (µA/µm)							
	UTB FD (µA/µm)	1.1E-05	1.1E-05	1.2E-05	1.2E-05	1.2E-05	1.30E-05	1.60E-05
	DG (µA/µm)	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05
I_{Dsat}: NMOS drive current	$I_{d,sat}$: effective NMOS Drive Current [9]							
	Extended Planar Bulk (µA/µm)							
	UTB FD (µA/µm)	773	882	1016	1108	1188	1289	1392
	DG (µA/µm)	825	863	908	1011	1090	1192	1283

ITRS – Low Dynamic Power (I)

Process Integration - Devices

		2005	2006	2007	2008	2009	2010	2011	2012	2013
Year	*Year in Production*									
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
Technology node	*MPU Physical Gate Length (nm)*	32	28	25	22	20	18	16	14	13
Physical gate length (low dynamic power)	L_g: *Physical gate length for LOP (nm) [1]*	45	37	32	28	25	22	20	18	16
EOT: Equiv. oxide thickness	*EOT: Equivalent Oxide Thickness [2]*									
	Extended planar bulk (Å)	14	13	12	11	10	9	9	9	
	UTB FD (Å)							9	9	8
	DG (Å)							9	9	8
V_{DD}: power supply	V_{dd}: *Power Supply Voltage (V) [6]*	0.9	0.9	0.8	0.8	0.8	0.7	0.7	0.7	0.6
V_{tsat}: Saturation threshold voltage	$V_{t,sat}$: *Saturation Threshold Voltage [7]*									
	Extended Planar Bulk (mV)	288	303	285	271	276	226	233	231	
	UTB FD (mV)							273	268	272
	DG (mV)							261	255	257
I_{off}: S/D subthreshold leakage current	$I_{sd,leak}$: *Source/Drain Subthreshold Off-State Leakage Current [8]*									
	Extended Planar Bulk (µA/µm)	3.00E-03	3.00E-03	5.00E-03	8.6E-03	8.0E-03	5.00E-03	1.80E-02	2.50E-02	
	UTB FD (µA/µm)							8.00E-03	1.00E-02	1.00E-02
	DG (µA/µm)							5.00E-03	7.00E-03	7.00E-03
I_{Dsat}: NMOS drive current	$I_{d,sat}$: *effective NMOS Drive Current [9]*									
	Extended Planar Bulk (µA/µm)	589	607	573	612	652	749	749	774	
	UTB FD (µA/µm)							740	765	718
	DG (µA/µm)							783	822	789

ITRS – Low Dynamic Power (II)

Process Integration - Devices

		2014	2015	2016	2017	2018	2019	2020
Year	*Year in Production*							
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
Technology node	*MPU Physical Gate Length (nm)*	11	10	9	8	7	6	6
Physical gate length (low dynamic power)	L_g: *Physical gate length for LOP (nm) [1]*	14	13	11	10	9	8	7
EOT: Equiv. oxide thickness	*EOT: Equivalent Oxide Thickness [2]*							
	Extended planar bulk (Å)							
	UTB FD (Å)	8	8	7				
	DG (Å)	8	8	7	7	7	7	7
V_{DD}: power supply	V_{dd}: *Power Supply Voltage (V) [6]*	0.6	0.6	0.5	0.5	0.5	0.5	0.5
V_{tsat}: Saturation threshold voltage	$V_{t,sat}$: *Saturation Threshold Voltage [7]*							
	Extended Planar Bulk (mV)							
	UTB FD (mV)	275	277	254				
	DG (mV)	250	251	238	239	242	243	246
I_{off}: S/D subthreshold leakage current	$I_{sd,leak}$: *Source/Drain Subthreshold Off-State Leakage Current [8]*							
	Extended Planar Bulk (µA/µm)							
	UTB FD (µA/µm)	1.0E-02	1.0E-02	2.5E-02				
	DG (µA/µm)	1.0E-02	1.0E-02	2.0E-02	2.0E-02	2.0E-02	2.0E-02	2.0E-02
I_{Dsat}: NMOS drive current	$I_{d,sat}$: *effective NMOS Drive Current [9]*							
	Extended Planar Bulk (µA/µm)							
	UTB FD (µA/µm)	738	796	695				
	DG (µA/µm)	829	892	760	820	873	929	931

ITRS – Memory Technology

Process Integration - Devices

	Year in Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
Year / DRAM pitch	DRAM ½ Pitch (nm) [1]	80	70	65	57	50	45	40	35	32
	DRAM cell size (μm^2) [2]	0.0514	0.0408	0.0324	0.0193	0.0153	0.0122	0.0096	0.0077	0.0061
EOT: Capacitor equiv. oxide thickness	DRAM storage node cell capacitor dielectric: equivalent oxide thickness EOT (nm) [3]	1.8	1.4	1.1	0.9	0.8	0.6	0.6	0.5	0.5
DRAM capacitor voltage	DRAM storage node cell capacitor voltage (V) [4]	1.5	1.4	1.3	1.2	1.1	1.1	1.1	1	1
	Electric field of capacitor dielectric, (MV/cm) [5]	8	10	12	13	14	18	18	20	20
	DRAM cell FET dielectric: equivalent oxide thickness, EOT (nm) [6]	5.5	5	5	4.5	4	4	4	4	4
Max. worline level	Maximum Wordline (WL) level (V) [7]	3.5	3.3	3.3	3	2.7	2.7	2.7	2.6	2.6
	Electric field of cell FET device dielectric (MV/cm) [8]	6.4	6.6	6.6	6.7	6.8	6.8	6.8	6.5	6.5
	Cell Size Factor: a [9]	8	8	8	6	6	6	6	6	6
	Array Area Efficiency [10]	0.63	0.63	0.63	0.56	0.56	0.56	0.56	0.56	0.56
DRAM retention time	Minimum DRAM retention time (ms) [11]	64	64	64	64	64	64	64	64	64
DRAM soft error rate	DRAM soft error rate (fits) [12]	1000	1000	1000	1000	1000	1000	1000	1000	1000

	Year in Production	2014	2015	2016	2017	2018	2019	2020
Year / DRAM pitch	DRAM ½ Pitch (nm) [1]	28	25	22	20	18	16	14
	DRAM cell size (μm^2) [2]	0.0048	0.0038	0.0030	0.0024	0.0019	0.0015	0.0012
EOT: Capacitor equiv. oxide thickness	DRAM storage node cell dielectric: equivalent physical thickness EOT (nm) [3]	0.45	0.4	0.4	0.3	0.25	0.2	0.15
DRAM capacitor voltage	DRAM storage node capacitor voltage (V) [4]	1	0.9	0.9	0.7	0.7	0.7	0.7
	Electric field of capacitor dielectric, (MV/cm) [5]	22	23	23	23	28	35	47
	DRAM cell FET dielectric: equivalent oxide thickness, EOT (nm) [6]	4	3.5	3.5	3.5	3	3	3
Max. worline level	Maximum Wordline (WL) level (V) [7]	2.6	2.3	2.3	2.3	2	2	2
	Electric field of cell FET device dielectric (MV/cm) [8]	6.5	6.6	6.6	6.6	6.7	6.7	6.7
	Cell Size Factor: a [9]	6	6	6	6	6	6	6
DRAM retention time	Array Area Efficiency [10]	0.56	0.56	0.56	0.56	0.56	0.56	0.56
DRAM soft error rate	Minimum DRAM retention time (ms) [11]	64	64	64	64	64	64	64
	DRAM soft error rate (fits) [12]	1000	1000	1000	1000	1000	1000	1000

ITRS – Reliability

Process Integration - Devices

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
Year / DRAM pitch	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
Physical gate length	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
Early failures	Early failures (ppm) (First 4000 operating hours)** [1]	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
Long term failures	Long term reliability (FITS = failures in 1E9 hours) [2]	10-100	10-100	50–2000	10–100	10–100	10–100	10–100	10–100	10–100
Soft error rate	Soft error rate (FITs)	1000	1000	1000	1000	1000	1000	1000	1000	1000
	Relative failure rate per transistor (normalized to2005 value) [3]	1.00	0.79	0.63	0.50	0.40	0.32	0.25	0.20	0.16
	Relative failure rate per m of interconnect (normalized to2005 value) [4]	1.00	0.84	0.71	0.59	0.51	0.47	0.41	0.37	0.33

	Year of Production	2014	2015	2016	2017	2018	2019	2020
Year / DRAM pitch	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
Physical gate length	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
Early failures	Early failures (ppm) (First 4000 operating hours)** [1]	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
Long term failures	Long term reliability (FITS = failures in 1E9 hours) [2]	10–100	10–100	10–100	10–100	10–100	10–100	10–100
Soft error rate	Soft error rate (FITs)	1000	1000	1000	1000	1000	1000	1000
	Relative failure rate per transistor (normalized to2005 value) [3]	0.13	0.10	0.08	0.06	0.05	0.04	0.03
	Relative failure rate per m of interconnect (normalized to2005 value) [4]	0.29	0.27	0.22	0.20	0.18	0.16	0.14

ITRS – Design Challenges (I)

Design

Year	*Year of Production*	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Design Reuse	*Design Reuse*									
	Design block reuse [1] % to all logic size	32%	33%	35%	36%	38%	40%	41%	42%	44%
	Design block reuse [1] % to all logic size	32%	33%	35%	36%	38%	40%	41%	42%	44%
	Platforms supported [4] % of platforms fully supported by tools [5]	3%	6%	10%	25%	35%	50%	57%	64%	75%
	Platforms supported [4] % of platforms fully supported by tools [5]	3%	6%	10%	25%	35%	50%	57%	64%	75%
High Level Synthesis	*High Level Synthesis*									
	Accuracy of high level estimates (performance, area, power, costs) [6] % versus measurements	53%	56%	60%	63%	66%	70%	73%	76%	80%
Reconfigurability	*Reconfigurability*									
	SOC reconfigurability [7] % of SOC functionality reconfigurable	23%	26%	28%	28%	30%	35%	38%	40%	42%
	SOC reconfigurability [7] % of SOC functionality reconfigurable	23%	26%	28%	28%	30%	35%	38%	40%	42%
Analog/Mixed-Signal	*Analog/Mixed Signal*									
	Analog automation [8] % versus digital automation [9]	12%	14%	17%	17%	24%	24%	27%	30%	32%
	Analog automation [8] % versus digital automation [9]	12%	14%	17%	17%	24%	24%	27%	30%	32%
	Modeling methodology, description languages, and simulation environments [10] % versus digital methodology [11] [12]	53%	55%	58%	60%	62%	65%	67%	70%	73%

ITRS – Design Challenges (II)

Design

Year	*Year of Production*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Design Reuse	*Design Reuse*							
	Design block reuse [1] % to all logic size	46%	48%	49%	51%	52%	54%	55%
	Design block reuse [1] % to all logic size	46%	48%	49%	51%	52%	54%	55%
	Platforms supported [4] % of platforms fully supported by tools [5]	80%	85%	90%	92%	94%	95%	97%
	Platforms supported [4] % of platforms fully supported by tools [5]	80%	85%	90%	92%	94%	95%	97%
High Level Synthesis	*High Level Synthesis*							
	Accuracy of high level estimates (performance, area, power, costs) [6] % versus measurements	83%	86%	90%	92%	94%	95%	97%
Reconfigurability	*Reconfigurability*							
	SOC reconfigurability [7] % of SOC functionality reconfigurable	45%	48%	50%	53%	56%	60%	62%
	SOC reconfigurability [7] % of SOC functionality reconfigurable	45%	48%	50%	53%	56%	60%	62%
Analog/Mixed-Signal	*Analog/Mixed Signal*							
	Analog automation [8] % versus digital automation [9]	35%	38%	40%	43%	46%	50%	52%
	Analog automation [8] % versus digital automation [9]	35%	38%	40%	43%	46%	50%	52%
	Modeling methodology, description languages, and simulation environments [10] % versus digital methodology [11] [12]	76%	78%	80%	83%	86%	90%	92%

ITRS – Design Challenges (III)

Design

Year	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
Asynchronous global signaling	Asynchronous global signaling % of a design driven by handshake clocking	5%	5%	7%	11%	15%	17%	19%	20%	22%
	Parameter uncertainty %-effect (on sign-off delay)	5%	6%	6%	8%	10%	11%	11%	12%	14%
	Simultaneous analysis objectives # of objectives during optimization	4	4	4	5	6	6	6	6	7
MTTF – Reliability factor	MTTF contribution reliability factor	1	1.1	1.2	1.3	1.4	1.6	1.7	1.8	1.9
Circuit families	Circuit families # of circuit families in a single design	2	2	3	3	4	4	4	4	4
Analog content synthesized	Analog content synthesized % of a design	10%	13%	15%	16%	17%	18%	19%	20%	23%
	Leakage # times per device	2	3	4	6	8	9.5	11	12	14

Year	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
Asynchronous global signaling	Asynchronous global signaling % of a design driven by handshake clocking	20%	25%	30%	30%	30%	35%	40%
	Parameter uncertainty %-effect (on sign-off delay)	15%	18%	20%	20%	20%	22%	25%
	Simultaneous analysis objectives # of objectives during optimization	8	8	8	8	8	8	8
MTTF – Reliability factor	MTTF contribution reliability factor	2	2.1	2.2	2.3	2.5	2.6	2.7
Circuit families	Circuit families # of circuit families in a single design	4	4	4	4	4	4	4
Analog content synthesized	Analog content synthesized % of a design	25%	28%	30%	35%	40%	45%	50%
	Leakage # times per device	16	24	32	32	32	32	32

ITRS – Design for Test (I)

Design

Year	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
Analog/Mixed-Signal/RF	System Driver: Analog/Mixed-signal RF									
All digital DFT for analog/mixed-signal/RF	1. All-digital DFT for analog mixed-signal/RF circuits and systems % digital circuits in DFT implementations	30	35	40	45	50	55	60	60	60
	2. Correlation of DFT results with existing specification-based test methods. % results correlated	30	35	40	45	50	55	60	60	60
Availability of fault/defect models for AMS/RF	3. Availability of fault/defect models for DFT-oriented test methods. % AMS/RF blocks with accepted fault models	20	20	25	30	35	40	45	50	55
MPU/DSP	System Drivers: MPU/PE/DSP/									
DFT coverage	1. DFT coverage of digital blocks or subsystems. % blocks with DFT	60	60	70	70	70	75	75	75	80
Critical paths delay fault coverage	2. DFT for delay test of critical paths. % paths covered	50	50	55	55	60	60	60	60	70
Blocks with DFT for fault tolerance	3. DFT for fault tolerance in logic blocks. % blocks with fault tolerance	40	40	40	40	45	45	50	50	55
Memories	System Drivers: Memories									
DFT for yield improvement	1. DFT for yield improvement.	85	85	85	90	90	90	90	95	95
SOC/SIP	General SOC/SIP requirements									
DFT support for logic repair	1. DFT-support for logic and other circuit repair (except memory). % blocks with repair	50	50	50	60	60	60	70	70	70
DFT reuse for performance calibration	2. DFT re-use for performance calibration, and measurement purposes. % DFT circuits re-used	30	30	35	35	40	40	40	45	45
DFT impact on system performance	3. DFT impact on system performance (noise, power, sensitivity, bandwidth, etc.). % performance impact (aggregate figure of merit)	15	15	15	15	10	10	10	10	10
Test volume reduction	4. DFT efficacy in test volume reduction. reduction magnitude	2×	2×	5×	5×	5×	10×	10×	10×	20×
DFT – ATE interface standardization	5. DFT / ATE interface standard, including DFT control via standard test access protocols. % of test interface standardized	40	40	45	45	50	50	60	60	70

ITRS – Design for Test (II)

Design

Year
Analog/Mixed-Signal/RF
All digital DFT for analog/mixed-signal/RF
Availability of fault/defect models for AMS/RF
MPU/DSP
DFT coverage
Critical paths delay fault coverage
Blocks with DFT for fault tolerance
Memories
DFT for yield improvement
SOC/SIP
DFT support for logic repair
DFT reuse for performance calibration
DFT impact on system performance
Test volume reduction
DFT – ATE interface standardization

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
System Driver: Analog/Mixed-signal/RF							
1. All-digital DFT for analog/mixed-signal/RF circuits and systems. % digital circuits in DFT implementations	60	80	85	90	90	100	100
2. Correlation of DFT results with existing specification-based test methods. % results correlated	60	80	85	90	90	100	100
3. Availability of fault/defect models for DFT-oriented test methods. % % AMS/RF blocks with accepted fault models	60	65	70	75	80	85	90
System Drivers: MPU/PE/DSP							
1. DFT coverage of digital blocks or subsystems % blocks with DFT	80	85	85	90	90	95	95
2. DFT for delay test of critical paths. % paths covered	70	70	80	80	90	90	100
3. DFT for fault tolerance in logic blocks. % blocks with fault tolerance	55	60	65	70	80	90	100
System Drivers: Memory							
1. DFT for yield improvement.	95	95	98	98	98	100	100
General SOC/SIP requirements							
1. DFT-support for logic and other circuit repair (except memory). % blocks with repair	80	80	80	90	90	100	100
2. DFT re-use for performance calibration, and measurement purposes. % DFT circuits re-used	50	50	60	60	70	70	70
3. DFT impact on system performance (noise, power, sensitivity, bandwidth, etc.). % performance impact (aggregate figure of merit)	10	10	5	5	5	5	5
4. DFT efficacy in test volume reduction. reduction magnitude	20×	20×	20×	50×	50×	50×	50×
5. DFT / ATE interface standard, including DFT control via standard test access protocols. % of test interface standardized	70	75	90	80	90	100	100

ITRS – Design for Manufacturability

Design

Year
Mask cost
VDD variability
Vth variability
Circuit performance variability
Circuit power variability

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	
Mask cost ($m) from publicly available data	1.5	2.2	3.0	4.5	6.0	9.0	12.0	18.0	24.0	SOC
% V_{dd} Variability % variability seen at on-chip circuits	10%	10%	10%	10%	10%	10%	10%	10%	10%	SOC
% V_{th} variability Doping Variability impact on VTH	24%	29%	31%	35%	40%	40%	40%	58%	58%	SOC
% V_{th} variability Includes all sources	26%	29%	33%	37%	42%	42%	42%	58%	58%	SOC
% CD variability CD for now, might add doping later	12%	12%	12%	12%	12%	12%	12%	12%	12%	SOC
% circuit performance variability circuit comprising gates and wires	41%	42%	45%	46%	49%	50%	53%	54%	57%	SOC
% circuit power variability circuit comprising gates and wires	55%	55%	56%	57%	57%	58%	58%	59%	59%	SOC

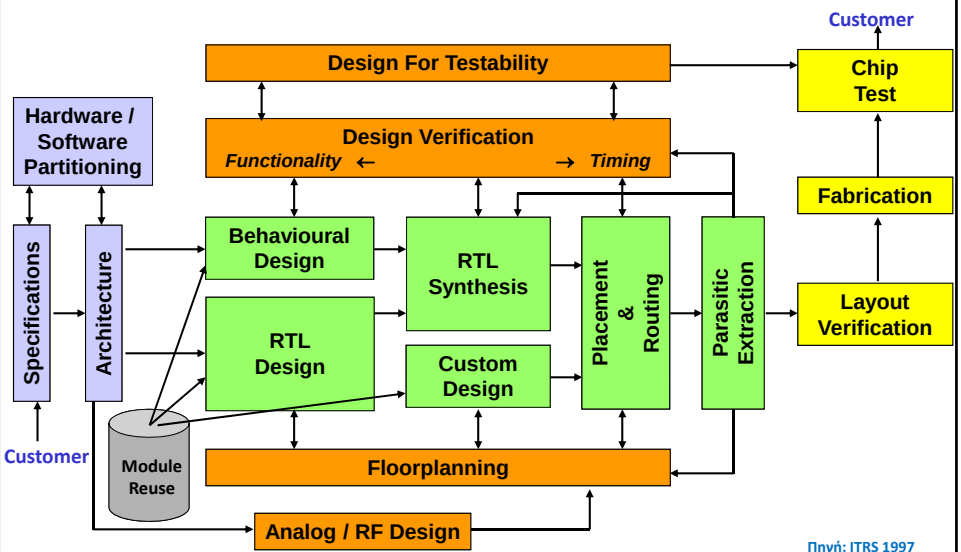
Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	
Mask cost ($m) from publicly available data	36.0	48.0	72.0	96.0	144.0	192.0	288.0	SOC
% V_{dd} Variability % variability seen at on-chip circuits	10%	10%	10%	10%	10%	10%	10%	SOC
% V_{th} variability Doping Variability impact on VTH	81%	81%	81%	81%	112%	112%	112%	SOC
% V_{th} variability Includes all sources	81%	81%	81%	81%	112%	112%	112%	SOC
% CD variability CD for now, might add doping later	12%	12%	12%	12%	12%	12%	12%	SOC
% circuit performance variability circuit comprising gates and wires	58%	61%	62%	65%	66%	69%	69%	SOC
% circuit power variability circuit comprising gates and wires	59%	60%	60%	61%	61%	62%	62%	SOC

ITRS – Additional Requirements

Design

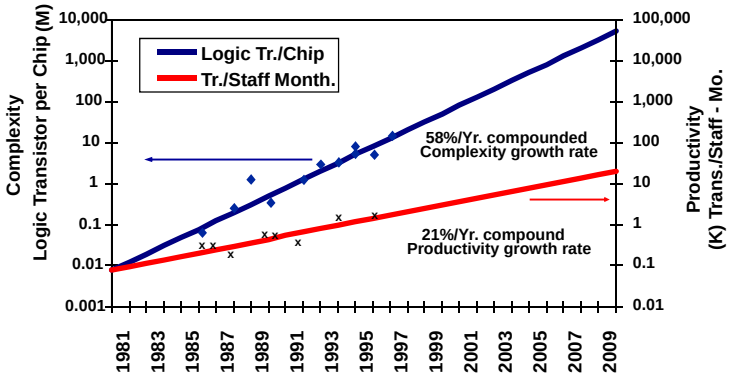
	Year of Production	2005	2006	2007	2008	2009	2012	2015	2018	Driver
	DRAM ½ Pitch (nm)	80	70	65	57	50	36	25	18	
SOC new design cycle	SOC new design cycle (months)	12	12	12	12	11	11	10	9	SOC
SOC logic per designer-year (10)	SOC logic Mtx per designer-year (10-person team)	3.3	4.3	5.4	7.4	10.6	24.6	73.4	113	SOC
SOC dynamic power reduction	SOC dynamic power reduction beyond scaling (X)	0.1	0.2	0.2	0.2	0.2	6	4.7	8.1	SOC
SOC standby power reduction	SOC standby power reduction beyond scaling (X)	2.4	3.4	5.1	6.4	8.73	18.8	44.4	232	SOC
Test coverage by BIST	% Test covered by BIST	25	30	35	40	45	60	75	90	MPU, SOC

Integrated Circuits Design Flow



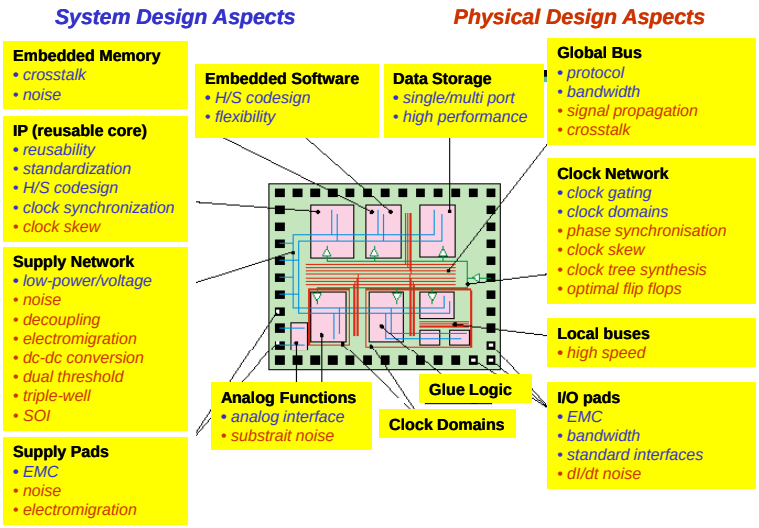
Πηγή: ITRS 1997

Complexity and Productivity

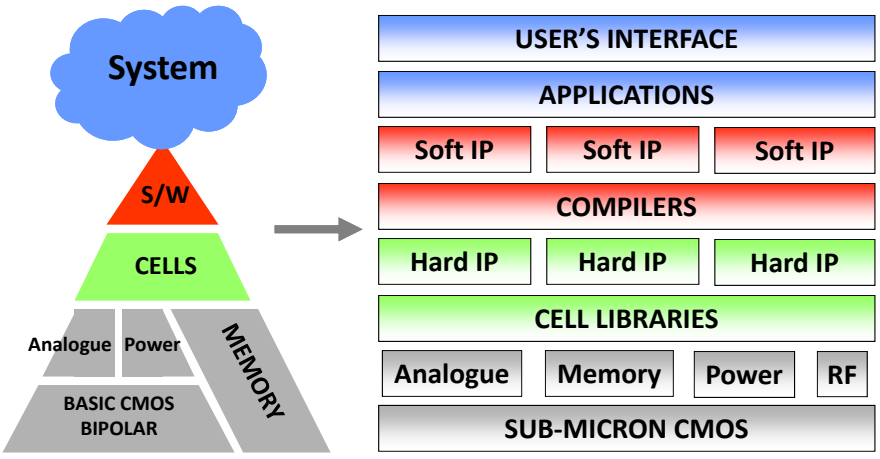


Πηγή: Sematech

SoC Design Aspects



Levels of Abstraction



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