TECHNICAL REPORT

On the Design of a Negative Voltage Conversion Circuit

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Abstract

In this work a new embedded negative voltage level converter is presented. The proposed circuit converts a positive input signal to a negative output signal obtaining an increased protection by the high voltage stress on the used MOS devices. This results in higher system reliability in applications where negative pulses are required. The circuit has been designed in a 0.18μm triple-well standard CMOS technology and simulation results are provided to demonstrate the efficiency of the proposed topology.

Index Terms – Embedded negative voltage level converter, level shifter, level conversion, MOS devices reliability.

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I. Introduction

Today, there is an increased demand for the use of multiple voltage levels in various semiconductor circuits like non-volatile memories [1-3], dynamic random access memories [4, 5], low power [6, 7], and low voltage [8] circuits. High voltages, above the nominal technology voltage, and negative voltages are widely used in circuit operation along with the nominal power supply voltage V_{DD}. For that reason, level conversion circuits, which convert a voltage level signal into another voltage level signal, are required for the proper interconnection between blocks with different operating voltages. Since negative voltages are exploited in many circuit operations (Flash memory erase operation [3, 9], DRAM refresh time enhancement [4, 5], low standby power consumption mode activation [6] e.t.c.) converters that can treat negative voltages are of great importance.

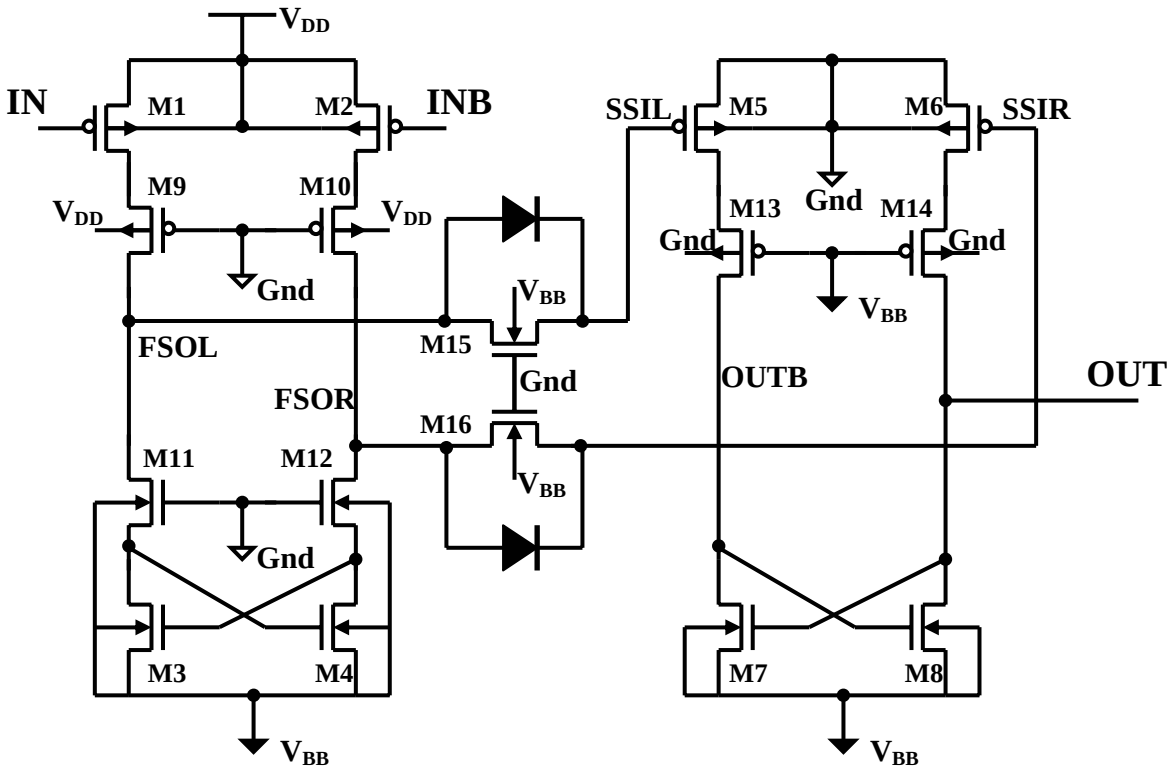
A negative level converter (NLC) is a circuit that converts a positive input signal (that is a signal with swing from Gnd (ground) to a positive voltage V_{DD}) into a negative output signal (that is a signal with swing from Gnd to a negative voltage V_{BB}). In the open literature, few level converters have been proposed [3-4] and [10-12] that convert a positive input signal to a signal with swing from a negative voltage V_{BB} to a positive voltage V_{PP}, where $V_{PP} \geq V_{DD}$. These structures, also called high/low level converters, require special high voltage devices and cannot be exploited, without modifications, in the design of an NLC circuit.

A feedback-type level conversion circuit is proposed in [4]. This converter requires additional low threshold voltage (low-V_t) high voltage transistors and thus it is not a cost attractive solution. Next in [10] a two stages level converter is presented, which consists of two cascaded converters. The first stage converts the input signal to a signal that swings between Gnd and V_{PP} and the second stage converts the output of the first stage to a signal that swings between V_{BB} and V_{PP}. A bootstrapped high/low level converted has been presented in [11]. This design presents a higher switching speed and a lower power operation than the previous one but it is not easily adaptable to very high voltage swings without performance loss and requires more silicon area. Finally, in [12] a level converter that is capable to operate efficiently at a lower than the nominal technology voltage (V_{DD}) has been proposed, while in [3] an improved version of this circuit for low voltage operation has been presented. However, as in the first case [4] the drawback of these two designs is that the technology must support dual threshold voltage (V_t) high voltage transistors. Note that, in all cases a triple well technology is required.

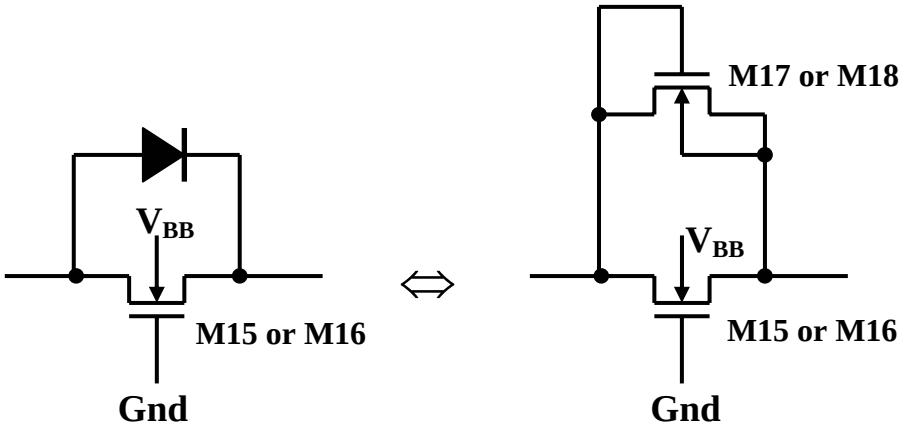
This work presents a negative voltage level conversion circuit with reduced voltage stress on its MOS devices, targeting applications of increased reliability where negative voltage pulses are needed. It is organised as follows. In Section II, the proposed negative level converter is described and its operation is analysed. Section III provides simulation results from the design of this converter in a 0.18μm CMOS technology. Finally, Section IV concludes this work.

II. The proposed negative level converter

Fig. 1(a) illustrates the proposed NLC circuit that targets to reduce the high voltage stress on the MOS devices when a positive input pulse is converted to a negative output pulse. It consists of two cascaded level converters. The first converter receives a signal with swing from Gnd to a positive voltage V_{DD} and provides a signal with swing from a negative voltage V_{BB} to V_{DD}. The second converter receives the output of the first converter (through a special protection topology as we will analyse next) and provides a signal with swing from V_{BB} to Gnd. Each level converter is based on cross-coupled transistor structures (transistors M3-M4 and M7-M8) that form a bi-stable circuit. The switching of nodes FSOL and FSOR as well as OUT and OUTB is a typical positive feedback process. Note that in either stable states there is no static current since transistors M1 and M4 or M2 and M3 as well as M5 and M8 or M6 and M7 are completely turned off.



(a)



(b)

Figure 1. The proposed negative level converter

The reduction of the high voltage stress in the proposed circuit is achieved with the use of extra transistors biased at proper, already existing, voltages. These transistors target the reduction of the voltage swing on the converter's internal lines in order to attain stress relaxation. In more details, transistors M9 and M10 biased at Gnd protect transistors M1 and M2 respectively by reducing the voltage swing at their drains [1]. Eliminating transistor M9 (M10) the maximum gate to drain voltage difference on M1 (M2) would be $V_{DD} + |V_{BB}|$, since when the gate voltage of M1 (M2) is V_{DD} (the transistor is in the cut-off region) its drain voltage is V_{BB}. The presence of M9 (M10) with its gate biased at Gnd results in a minimum voltage at the drain of M1 (M2) equal to $|V_{tp}|$ (where V_{tp} is the threshold voltage of the pMOS transistor) and thus a maximum gate to drain voltage difference equal to $V_{DD} - |V_{tp}|$. Consequently the voltage stress on M1 (M2) is reduced drastically. Moreover, the maximum gate to drain voltage difference on M9 (M10) is equal to $|V_{BB}|$ (considering that V_{DD} is the nominal technology voltage supply and usually $V_{DD}<|V_{BB}|$). The maximum gate to source voltage difference on M9 (M10) is equal to $V_{DD.}$ Finally, the maximum gate to substrate voltage difference in all cases above is equal to V_{DD}.

Similarly, transistors M11 and M12 biased also at Gnd protect transistors M3 and M4 respectively, while transistors M13 and M14 biased at V_{BB} protect transistors M5 and M6 respectively. In the first case, the maximum gate to drain voltage difference on M3 (M4) without and with M11 (M12) would be $V_{DD} + |V_{BB}|$ and $|V_{BB}|-V_{tn}$ respectively (where V_{tn} is the threshold voltage of the nMOS transistor). In addition, the maximum gate to drain or

gate to source voltage difference on M11 (M12) is equal to $|V_{BB}|$. In the second case (forgetting for the moment the combination of the diode connected transistor and pass transistor at the output of the first converter), the maximum gate to drain voltage difference on M5 (M6) without and with M13 (M14) would be $V_{DD} + |V_{BB}|$ and $V_{DD}+|V_{BB}-V_{tp}|$ respectively. Finally, the maximum gate to drain and gate to source voltage difference on M13 (M14) and M7 (M8) is equal to $|V_{BB}|$. In all cases above the maximum gate to substrate voltage difference is equal to $|V_{BB}|$.

A special structure is proposed for the interconnection of the two stages. It consists of a pass nMOS transistor with its gate biased at Gnd plus a diode connected nMOS transistor, as it is shown in Fig. 1(b). The pass transistor M15 (M16) establishes a voltage swing at the gate of transistor M5 (M6) from V_{BB} to $-V_{tn}$ and thus a further reduction to the maximum gate to drain voltage on the latter transistor is achieved equal to $|V_{BB}-V_{tp}|-V_{tn}$. Note that without this structure the voltage swing at the gate of M5 (M6) would be from V_{BB} to V_{DD}. Although a voltage equal to $-V_{tn}$ at the gate of M5 (M6) sets this transistor in the cut-off region, it contributes to a higher static leakage current consumption at the second stage with respect to a voltage equal to Gnd or higher. This inconvenience can be fixed using the diode-connected nMOS transistor M17 (M18), which raises the voltage swing at the gate of M5 (M6) and sets its range from V_{BB} to $V_{DD}-V_{tn}$. In that case, the maximum gate to drain voltage on M5 (M6) is equal to $V_{DD}-V_{tn}+|V_{BB}-V_{tp}|$. Assuming $|V_{BB}|>V_{DD}$, the maximum gate to source or drain or substrate voltage difference for the pass transistor is equal to $|V_{BB}|$, while for the diode connected transistor is equal to V_{tn}. .

Note that body effect phenomena increase the threshold voltage of the additional protection transistors resulting in better voltage stress relaxation in the NLC circuit. Consequently, under the above modifications we can set $|V_{BB}|$ up to the maximum allowable power supply voltage V_{max} of the used technology in case that the diode connected transistor is not used or set it equal to:

$$|V_{BB}| = V_{max} - V_{DD} + V_{tn} + |V_{tp}|$$

in case that the diode connected transistor is present.

In Fig. 2 a cross section view of the devices used in the design of the proposed NLC circuit and the peripheral CMOS logic are presented. Due to the use of a negative power supply (V_{BB}) where various transistor substrates are biased and the special structure of the diode connected transistor, a triple well technology should be exploited.

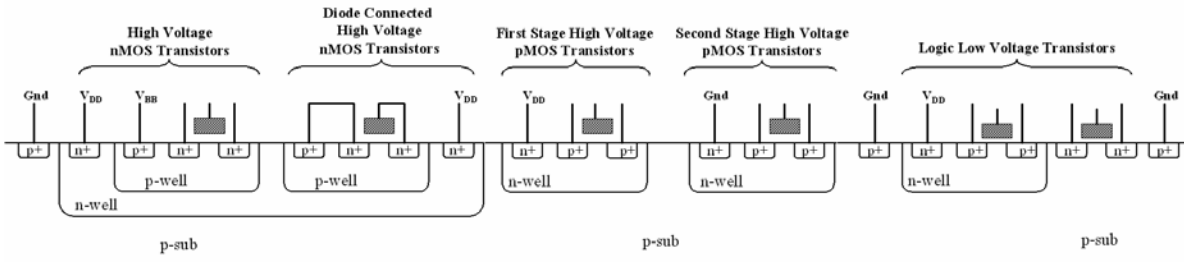


Figure 2. Cross section view

III. Circuit design issues and simulation results

The proposed negative level converter (incorporating the diode connected transistor) has been designed in the triple-well 0.18µm CMOS technology of ST-Microelectronics using high voltage (thick oxide) MOS transistors. These transistors are suited for 3.3V supply voltages (3.6V max power supply voltage). Although, the absolute maximum rating (AMR) is 4.0V, this stress affects the long term reliability of the device so that it is preferable not to exceed the 3.6V limit. The junction breakdown voltage is 10V. In addition, the nominal threshold voltages for the pMOS and nMOS devices are V_{tp}=-0.77V and V_{tn}=0.70V respectively, while the minimum channel length of a device is 0.36µm.

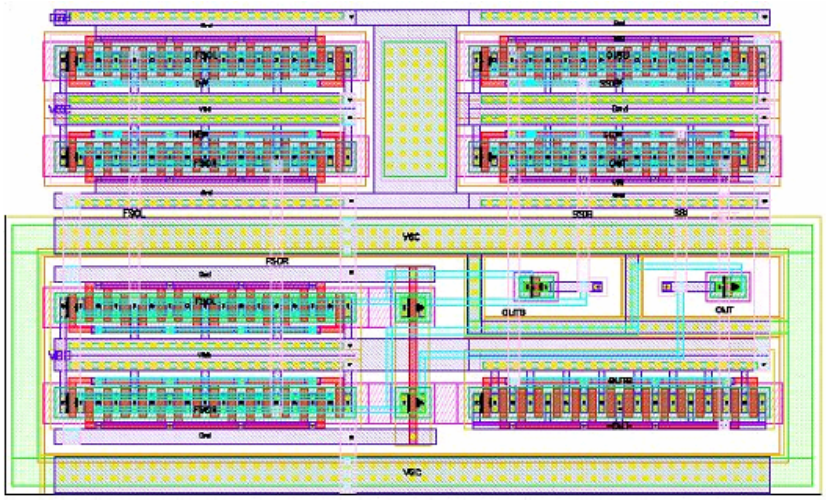


Figure 3. Layout view of the NLC circuit

The layout of the NLC circuit is shown in Fig. 3 covering an area of 37.16µm×24,36µm=905µm^2. The transistor sizes (W/L) are 8µm/0.36µm for the pMOS transistors of the first stage, 2µm/0.36µm for the nMOS transistors M11 and M12, 0.8µm/0.36µm the nMOS transistors M3 and M4, 5µm/0.36µm for the pMOS transistors

of the second stage and 0.8μm/0.36μm for the nMOS transistors of the second stage. Moreover, the sizes of the pass and the diode connected transistors are 1μm/0.36μm and 0.5μm/0.36μm respectively. The used power supply voltages were V_{BB}=-3.3V and V_{DD}=1.8V.

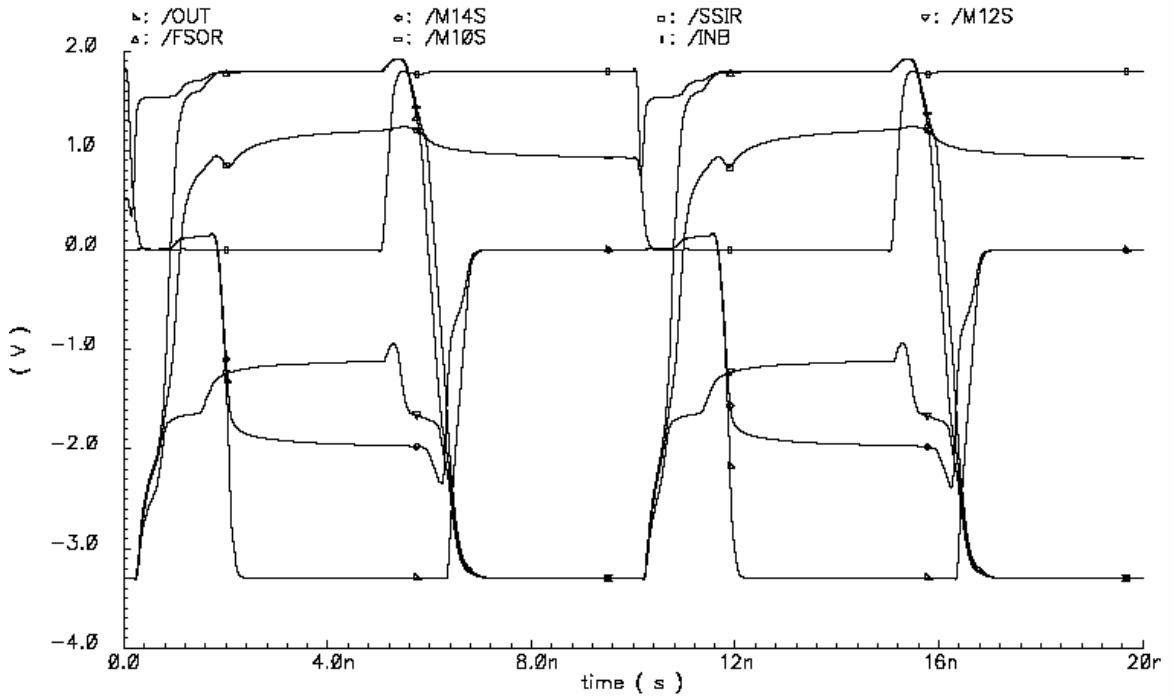


Figure 4. Simulated waveforms

According to electrical simulations, with SPECTRE, the voltage stress (gate to drain, gate to source or gate to substrate voltage difference) on any transistor in the design was less than or equal to 3.3V. Note that without the adopted protection mechanisms the voltage stress on the majority of the transistors in the design (M1-M6) would be equal to 5.1V. The corresponding waveforms at various nodes of the circuit, for a complete transition of the input signal *IN* from Gnd to V_{DD} and back to Gnd, are shown in Fig. 4. In more details, the waveforms at the source of the M10 transistor (equivalently the drain of M2 – see Fig. 1) and the *FSOR* node (right output of the first stage or M10 drain) are shown with respect to the complementary input signal *INB*. According to these results no voltage stress (outside the 3.6V technology limit) is observed on M2 and M10 transistors since the gate to source (or drain or substrate) voltage is less or equal to 3.3.V. Moreover, the waveform at the source of the M12 transistor (drain of the M4 transistor) is presented.

The voltage stress on transistors M4 and M12 is inside the limit, considering that the gate of M4 is fed by a signal that is complementary to this on its drain. In addition, the waveform at the *SSIR* node (second stage right input) is given. Obviously, the pass and the diode connected transistors are well protected against any excessive voltage stress. Finally, the waveforms at the source of M14 (drain of M6) and the NLC output (*OUT*) are shown. Once again the gate to source (or drain or substrate) voltage differences on transistors M6, M8 and M14 are well within the technology limits (considering that the gate of M8 is driven by the signal *OUTB* which is complementary to the *OUT* signal). Note that the waveforms at nodes *IN*, M9 source, *FSOL*, M11 source, *SSIL*, M13 source and *OUTB* are complementary to the waveforms in Fig. 4 and consequently no voltage stress is observed also on transistors M1, M3, M5, M7, M9, M11 and M13.

Finally, the delay of this NLC circuit is 1.82ns when it drives an inverter with a fan-in equal to this of its second stage, while the power consumption is 0.53mW.

IV. Conclusions

In this work a negative voltage level conversion circuit is presented. This circuit converts a positive digital signal to a negative one so that it can be exploited in applications where negative voltage pulses are required. The proposed topology provides increased protection to the used transistors against the high voltage stress that may arise across their terminals during the circuit operation. According to the simulation results derived from a level conversion circuit designed in a 0.18μm CMOS technology, the voltage stress on its MOS devices is drastically reduced (down to the nominal technology levels in our case) resulting in enhanced circuit reliability.

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