ΤΜΗΜΑ ΜΗΧΑΝΙΚΩΝ Η/Υ & ΠΛΗΡΟΦΟΡΙΚΗΣ • ΠΑΝΕΠΙΣΤΗΜΙΟ ΙΩΑΝΝΙΝΩΝ
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING • UNIVERSITY OF IOANNINA

ΠΑΡΟΥΣΙΑΣΗ
ΔΙΔΑΚΤΟΡΙΚΗΣ ΔΙΑΤΡΙΒΗΣ

ΗΜΕΡΟΜΗΝΙΑ: Παρασκευή, 4 Οκτωβρίου 2019

ΩΡΑ: 18:00

ΑΙΘΟΥΣΑ: Αίθουσα Σεμιναρίων
Κτήριο Τμήματος Μηχανικών Η/Υ & Πληροφορικής

ΟΜΙΛΗΤΗΣ: **Παναγιώτης Γεωργίου**

Θ έ μ α

«System-On-Chip Testing»

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Π ε ρ ί λ η ψ η

This research focuses in the development of new Test-Access-Mechanism (TAM) architectures and test-scheduling methods for 3D-Systems-on-Chips (3D-SoCs), which exploit the high speed offered by Through-Silicon-Vias (TVSs), while power and thermal constraints are met. We introduce new TAM architectures for 3D SoCs, which minimize the test-time, the number of TSVs, and TAM lines used for transferring test-data to the cores. The test schedules are generated by the means of very effective Time-Division-Multiplexing (TDM) methods and highly efficient optimization algorithms. Experiments have shown that significant test-time savings can be achieved using the proposed architectures, especially under strict power and thermal constraints. In addition we introduce the first fault-independent Software Based Self Test (SBST) method, which offers short test-program generation time for processors under strict test-application-time and test-program-size constraints. The test-programs are evaluated by means of a novel and very effective SBST-oriented probabilistic metric, which considers both the architectural model and the synthesized gate-level netlist of the design under test. The proposed metric, which is based on output deviations, is very fast as it omits the time-consuming functional fault-simulation, and it can be applied to any SBST-based method.

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