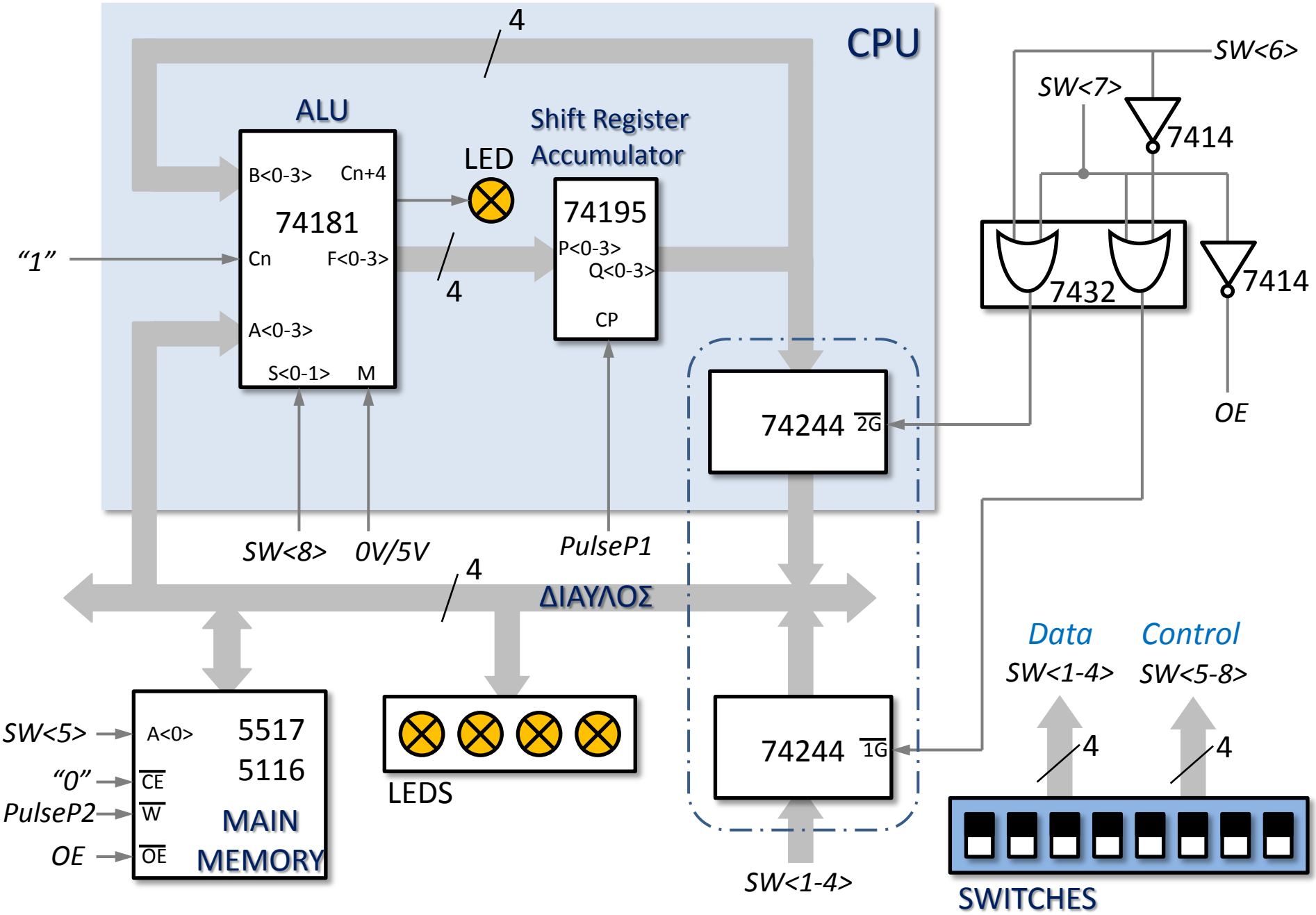
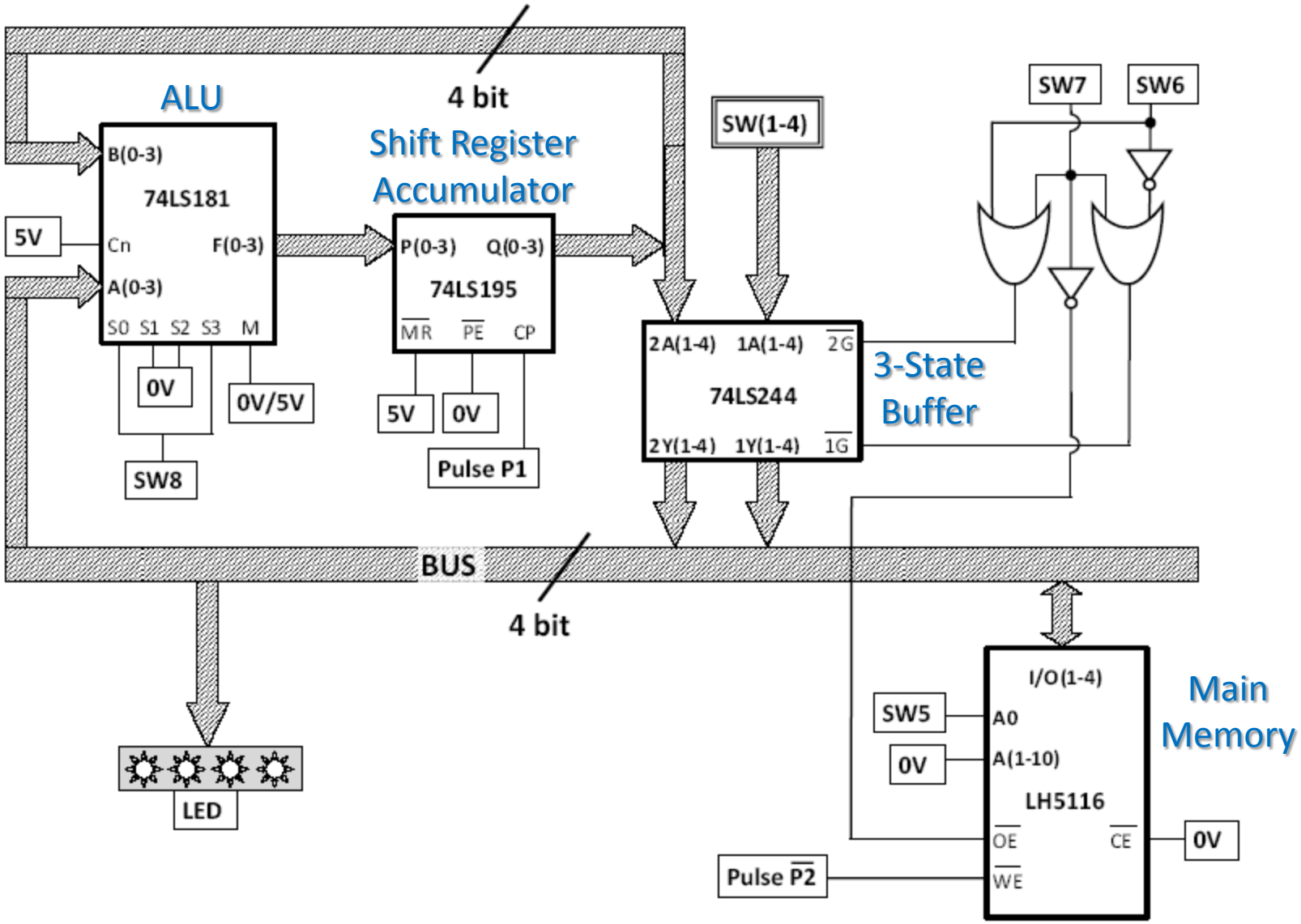
Εργαστήριο Τεχνολογίας Υλικού
και
Αρχιτεκτονικής Υπολογιστών

ΠΡΟΑΙΡΕΤΙΚΗ ΕΡΓΑΣΤΗΡΙΑΚΗ ΑΣΚΗΣΗ ΑΡΧΙΤΕΚΤΟΝΙΚΗΣ ΥΠΟΛΟΓΙΣΤΩΝ

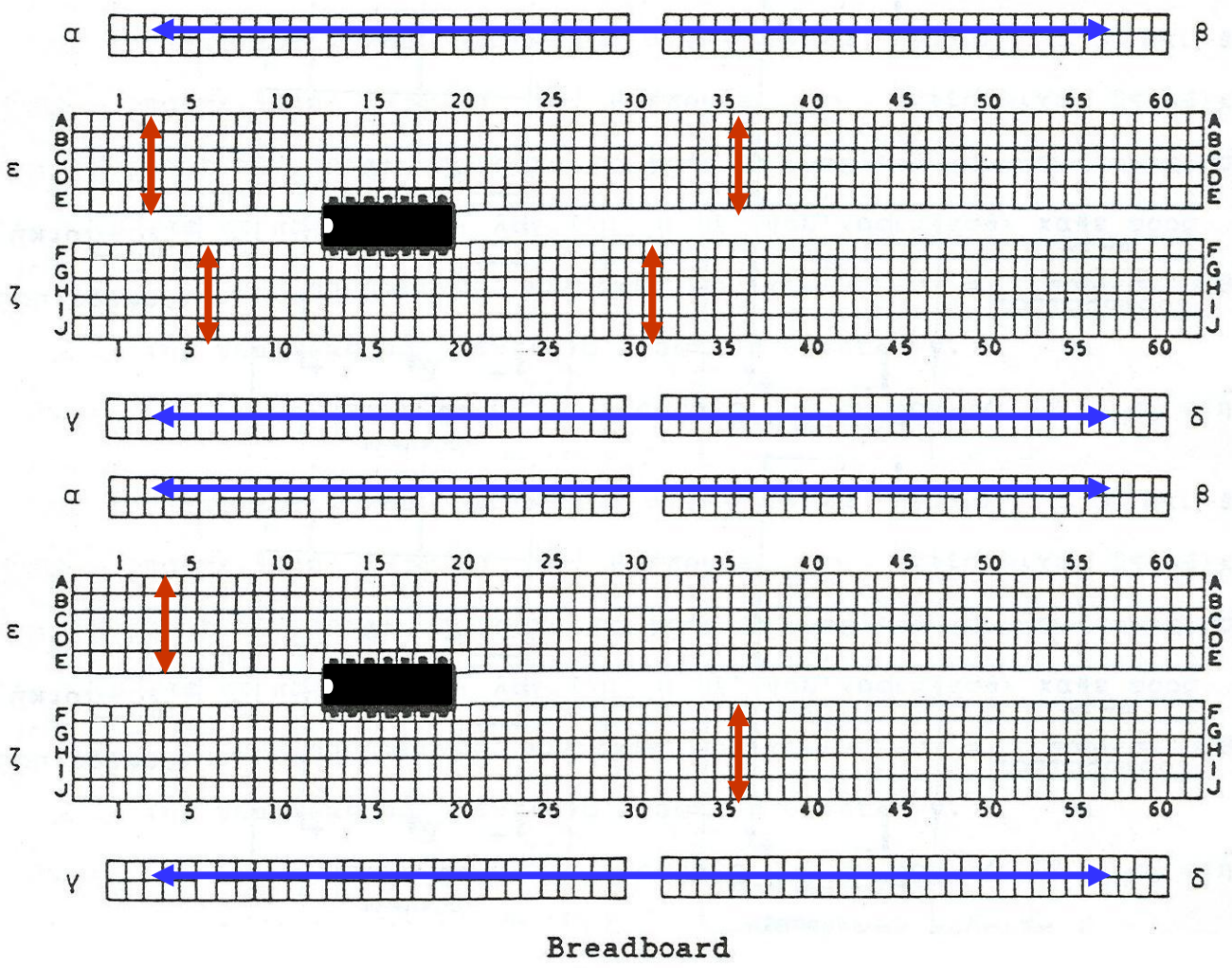
Σχεδίαση


CPU
ALU
74181
B<0-3>
Cn+4
Cn
F<0-3>
A<0-3>
S<0-1>
M
"1"
LED
Shift Register
Accumulator
74195
P<0-3>
Q<0-3>
CP
4
4
SW<8>
0V/5V
PulseP1
ΔΙΑΥΛΟΣ
4
74244 2G
74244 1G
SW<6>
SW<7>
7414
7432
7414
OE
Data
Control
SW<1-4>
SW<5-8>
4
4
SW<1-4>
SWITCHES
SW<5>
"0"
PulseP2
OE
A<0>
CE
W
OE
5517
5116
MAIN
MEMORY
LEDS

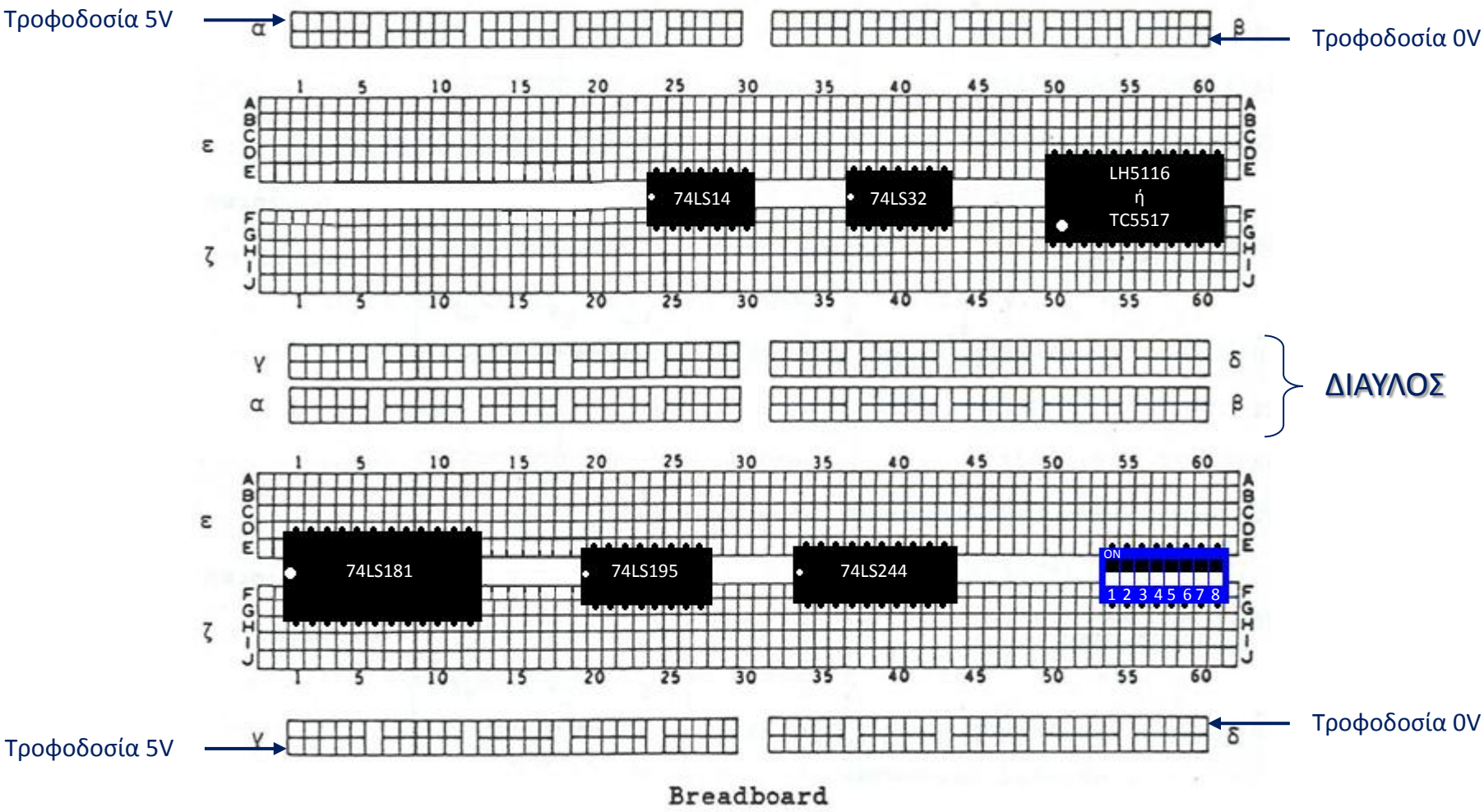
Σχεδίαση


ALU
4 bit
Shift Register
Accumulator
SW(1-4)
SW7
SW6
B(0-3)
74LS181
5V
Cn
F(0-3)
A(0-3)
S0 S1 S2 S3 M
0V
0V/5V
SW8
P(0-3) Q(0-3)
74LS195
MR PE CP
5V
0V
Pulse P1
2A(1-4) 1A(1-4) 2G
74LS244
2Y(1-4) 1Y(1-4) 1G
3-State
Buffer
BUS
4 bit
LED
I/O(1-4)
SW5
A0
0V
A(1-10)
LH5116
OE CE
0V
Pulse P2
WE
Main
Memory

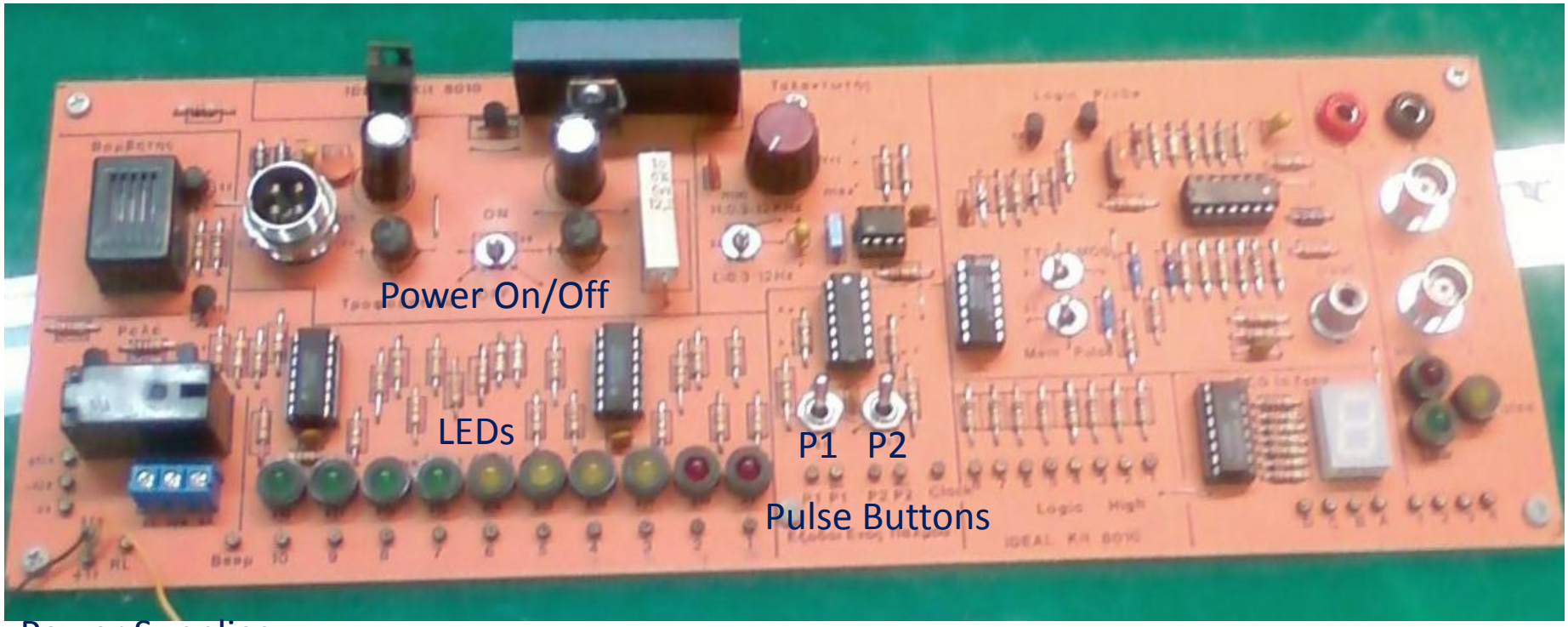
To Breadboard



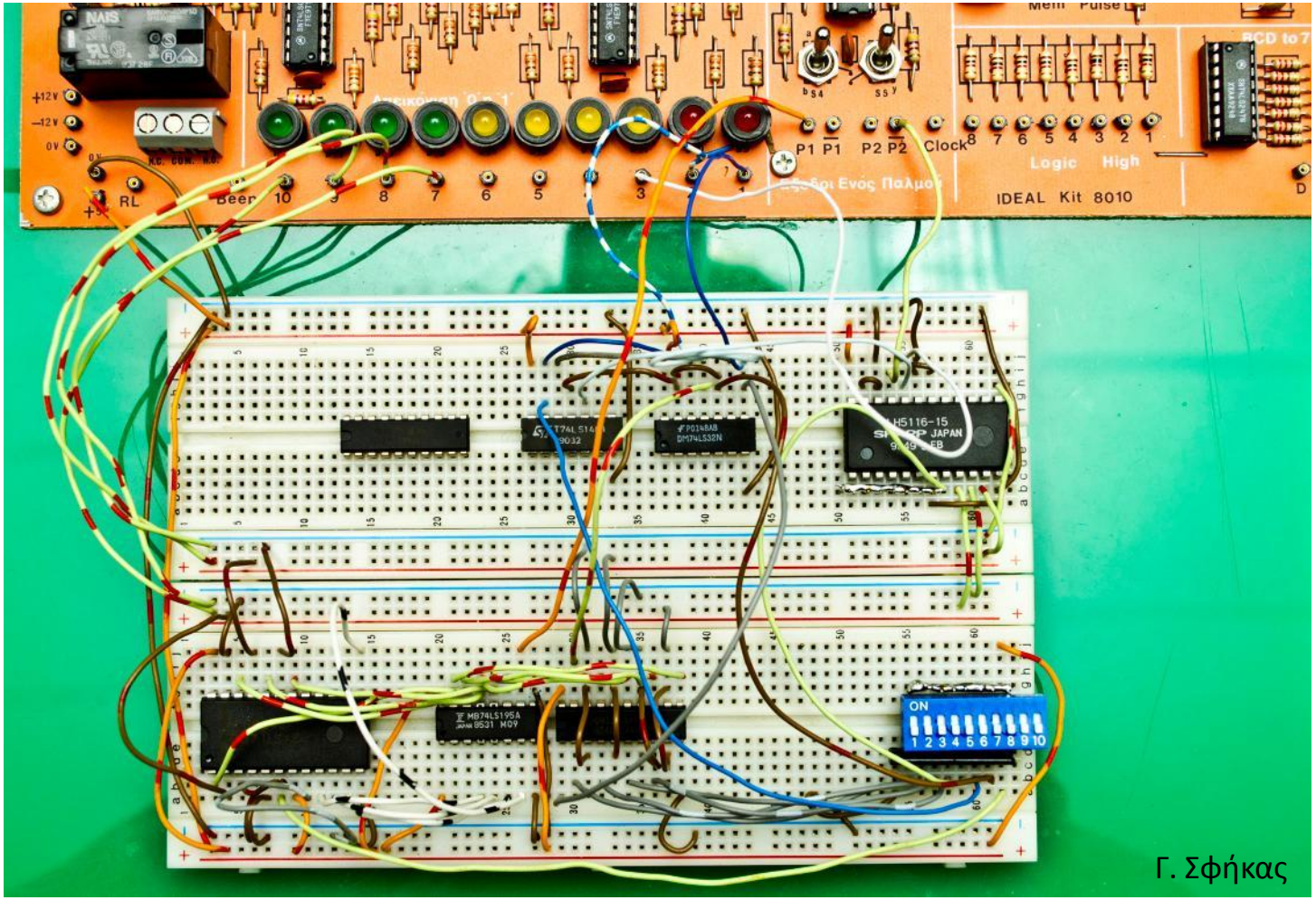
Τοπολογία Ολοκληρωμένων Κυκλωμάτων



Σύστημα Υποστήριξης



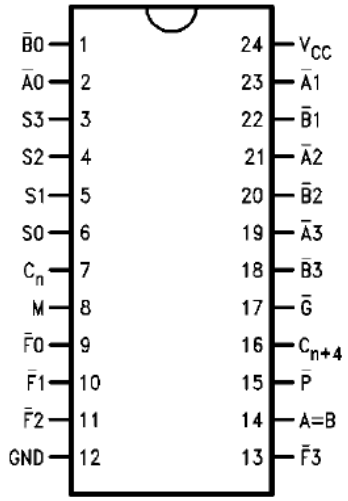
Υλοποίηση



Γ. Σφήκας

Arithmetic and Logic Unit (ALU) – 74LS181

Connection Diagram



Function Table

Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
				Logic	Arithmetic (Note 2)	Logic	Arithmetic (Note 2)
S3	S2	S1	S0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{A}\overline{B}$	AB minus 1	$\overline{A}+\overline{B}$	A + B
L	L	H	L	$\overline{A}+\overline{B}$	$A\overline{B}$ minus 1	$\overline{A}$ B	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A}+\overline{B}$	A plus (A + $\overline{B}$)	$\overline{A}\overline{B}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$\overline{A}\oplus\overline{B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}$ B	A plus (A + B)	$\overline{A}$ + B	A plus AB
H	L	L	H	A ⊕ B	A plus B	$\overline{A}\oplus\overline{B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A (Note 1)	Logic 1	A plus A (Note 1)
H	H	L	H	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

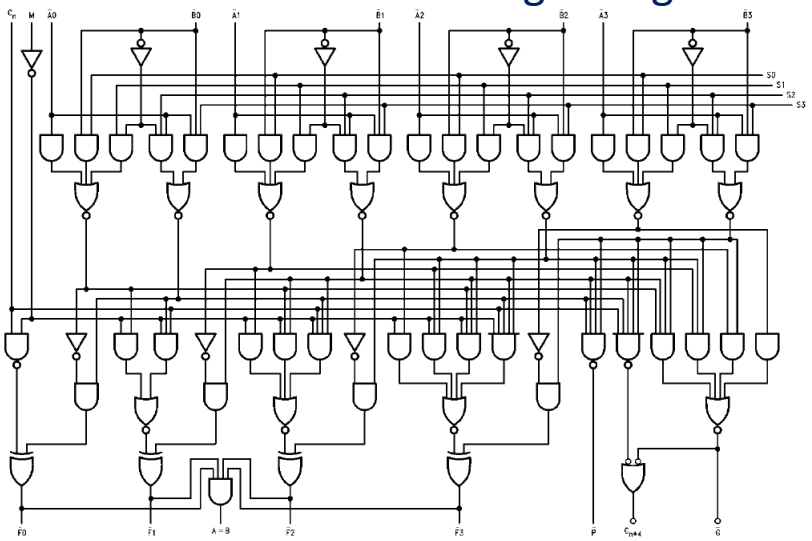
Note 1: Each bit is shifted to the next most significant position.

Note 2: Arithmetic operations expressed in 2s complement notation.

Pin Description

Pin Names	Description
$\overline{A}0$–$\overline{A}3$	Operand Inputs (Active LOW)
$\overline{B}0$–$\overline{B}3$	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}0$–$\overline{F}3$	Function Outputs (Active LOW)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

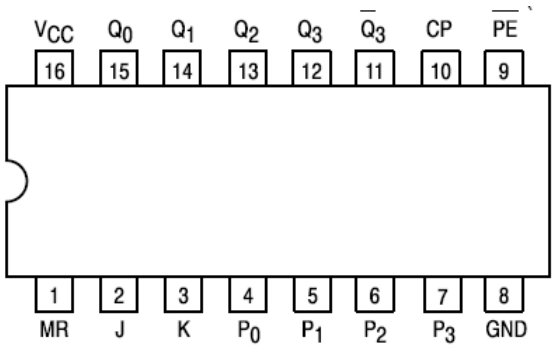
Logic Diagram



Οι αριθμητικές πράξεις είναι στο συμπλήρωμα ως προς 2

Shift Register – 74LS195

Connection Diagram

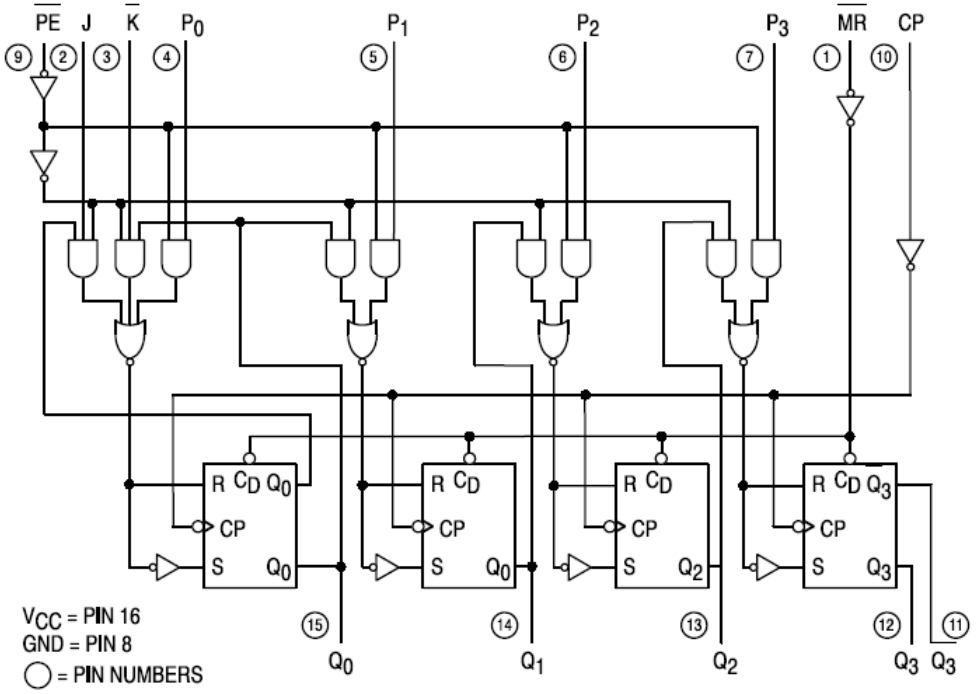


Truth Table

OPERATING MODES	INPUTS					OUTPUTS				
	MR	PE	J	K	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q_2}$
Shift, Reset First	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q_2}$
Shift, Toggle First Stage	H	h	h	l	X	q_0	q_0	q_1	q_2	$\overline{q_2}$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	q_2
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p_3}$

L = LOW voltage levels
H = HIGH voltage levels
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

Logic Diagram

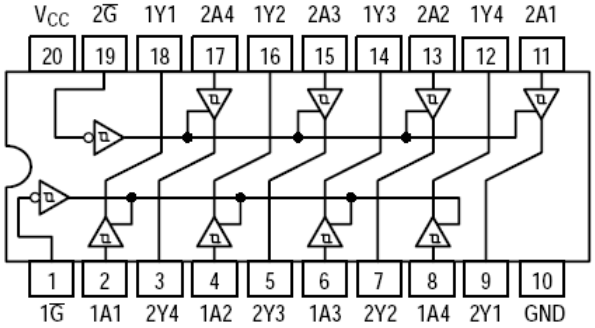


Pin Names

$\overline{PE}$	Parallel Enable (Active LOW) Input
$P_0 - P_3$	Parallel Data Inputs
$\underline{J}$	First Stage J (Active HIGH) Input
$\overline{K}$	First Stage K (Active LOW) Input
$\underline{CP}$	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$\underline{Q_0} - Q_3$	Parallel Outputs (Note b)
$\overline{Q_3}$	Complementary Last Stage Output (Note b)

3-State, Octal Buffer, Line Driver – 74LS244

Connection Diagram



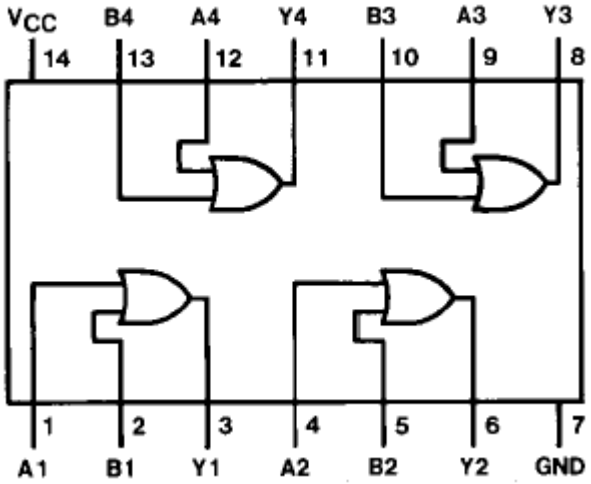
Truth Table

INPUTS		OUTPUT
$1\overline{G}$, $2\overline{G}$	D	
L	L	L
L	H	H
H	X	(Z)

OR Gates & NOT Gates – 74LS32 & 74LS14

OR

Connection Diagram



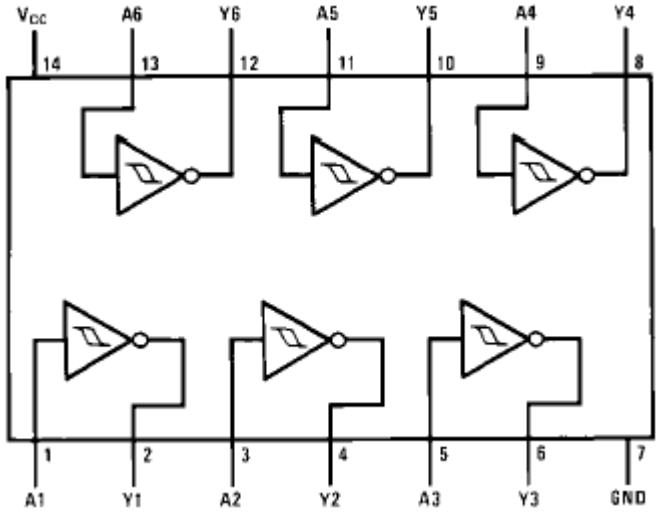
Truth Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

NOT

Connection Diagram



Truth Table

$Y = \overline{A}$

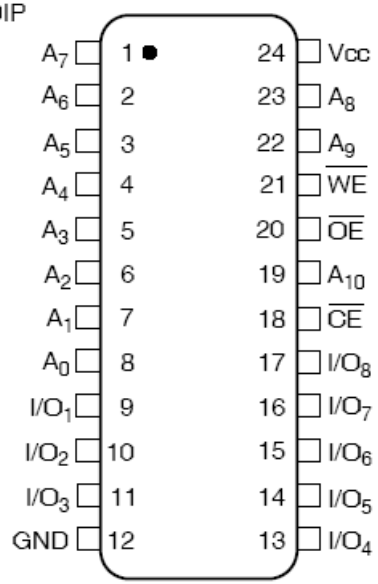
Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

SRAM – LH5116-H (2KB)

Connection Diagram

24-PIN DIP
24-PIN SK-DIP
24-PIN SOP

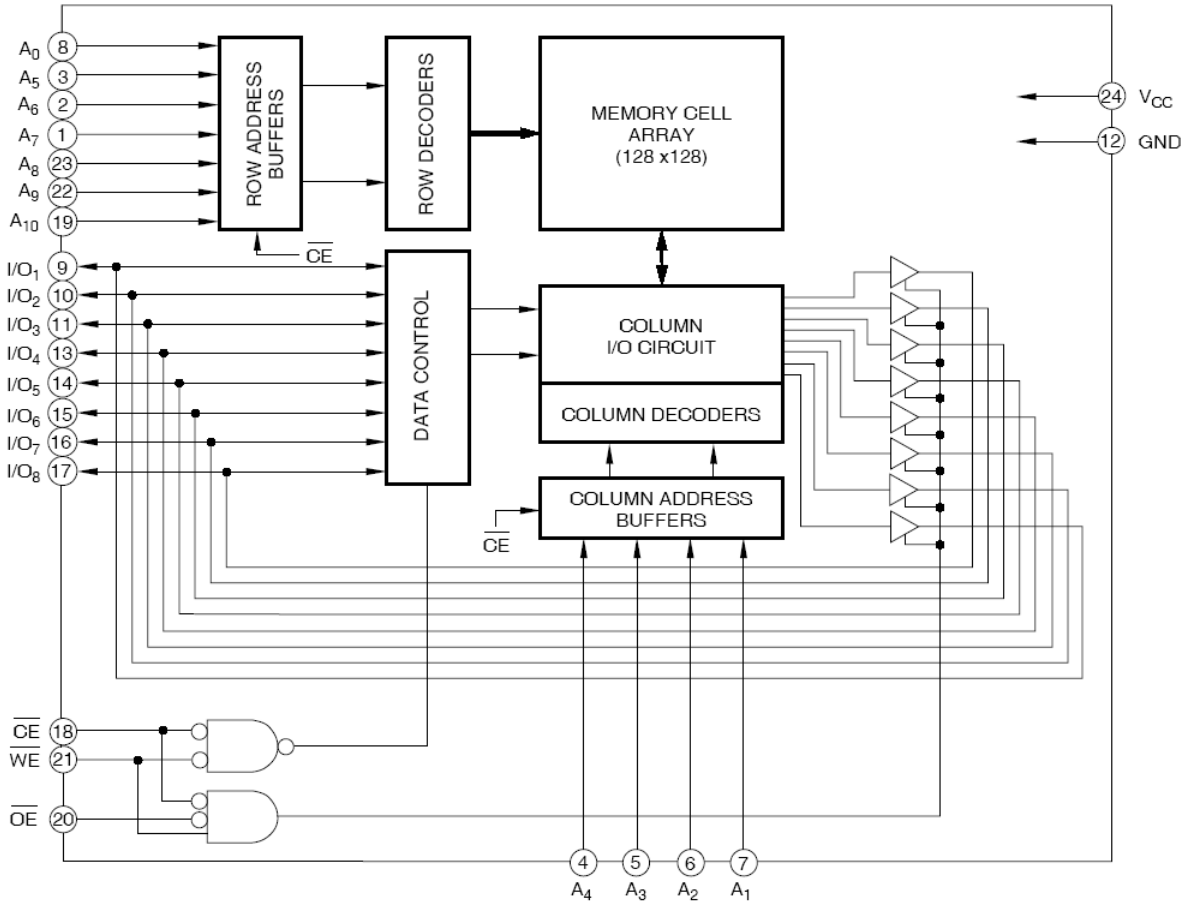


Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	X	L	Write	D_{IN}	Operating (ICC)	1
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	X	Outputs disable	High-Z	Operating (I_{CC})	1

NOTE:
1. X = H or L

Block Diagram



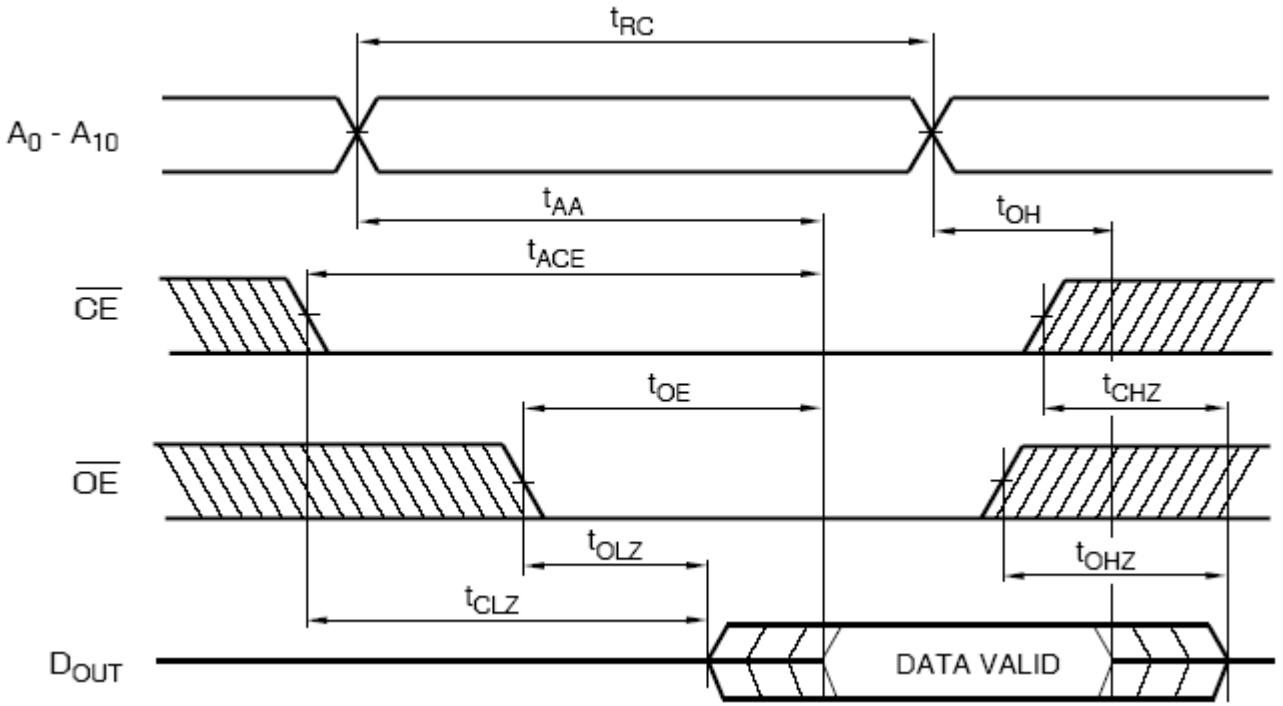
Pin Names

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground

SRAM – LH5116-H

Read Cycle

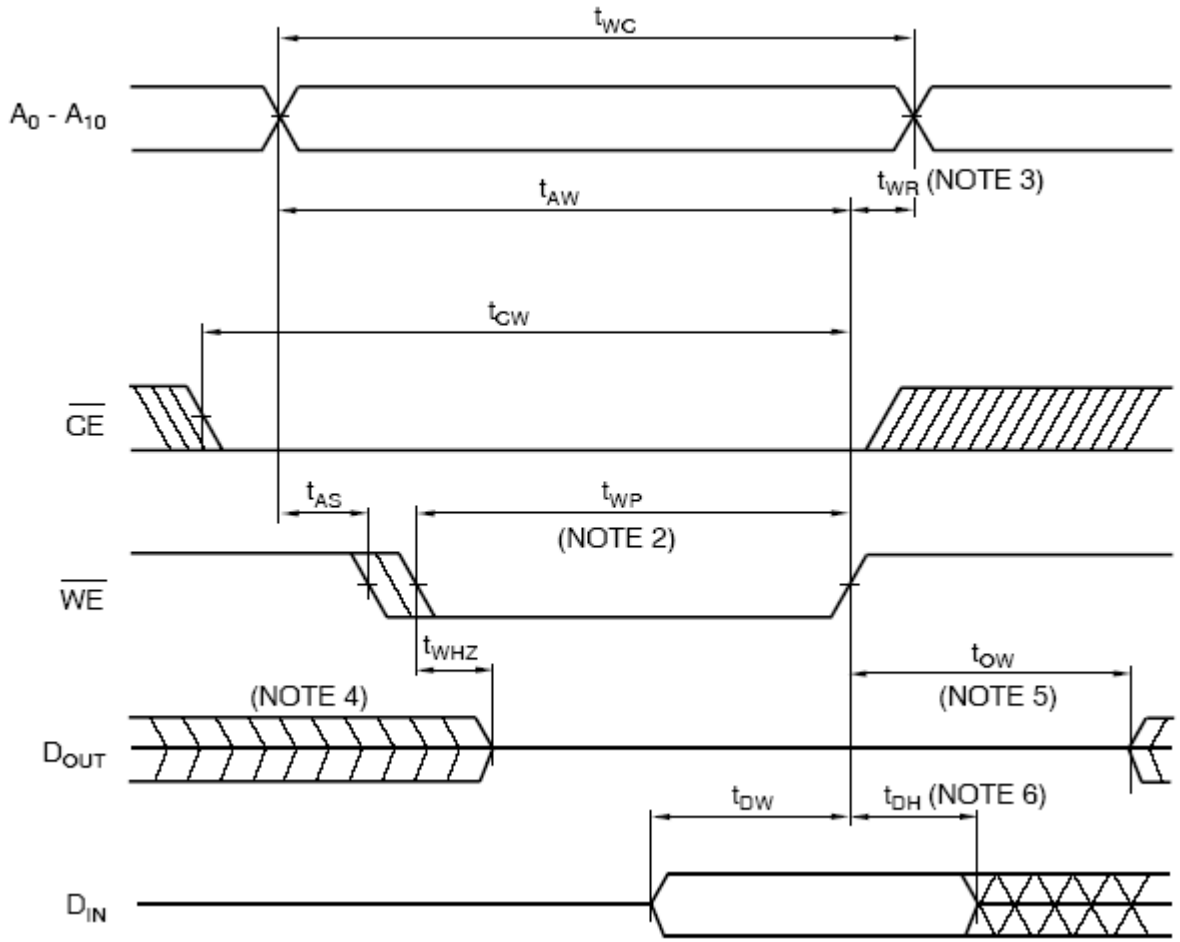


NOTE: $\overline{WE}$ = HIGH

SRAM – LH5116-H

Write Cycle – 1

NOTE: $\overline{OE}$ = HIGH

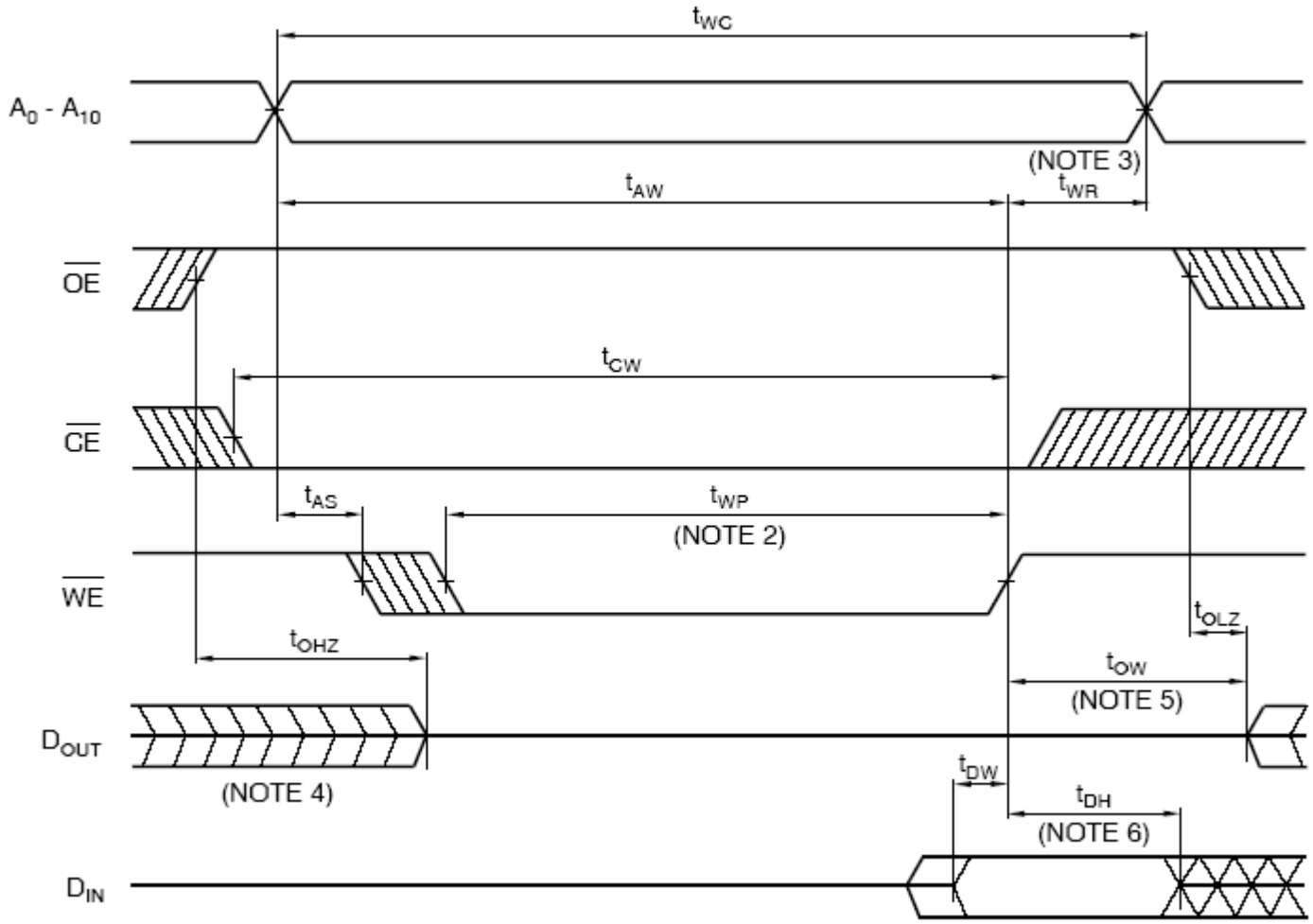


NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pin is in the output state. During this state, input signals of opposite logic level must not be applied.

SRAM – LH5116-H

Write Cycle – 2



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

Πίνακες

ΠΙΝΑΚΕΣ ΔΙΑΣΥΝΔΕΣΕΩΝ

Ο.Κ. Αναφοράς	# pin – Τύπος		Διασύνδεση με Ο.Κ.	# pin
74LS 195	1	I	Λογικό "1"	–
	2	I		
	3	I		
	4	I	74LS181	6
	5	I		
	6	I		
	7	I		
	8	T	Γείωση 0V	–
	9	I		
	10	I		
	11	O		
	12	O		
	13	O		
	14	O		
	15	O	74LS181 74LS244	1 11
	16	T	Τροφοδοσία 5V	–

Ο.Κ. = ολοκληρωμένο κύκλωμα, I=είσοδος, O=έξοδος, T=τροφοδοσία

Να δημιουργηθούν και να συμπληρωθούν οι πίνακες διασυνδέσεων και για τα έξη ολοκληρωμένα κυκλώματα.