KYKΛΩΜΑΤΑ VLSI

Processing Steps

From the book: An Introduction to VLSI Process
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ΚΥΚΛΩΜΑΤΑ VLSI

Διάρθρωση

1. Photolithography
2. Oxidation
3. Layer deposition
4. Etching
5. Diffusion
6. Implantation
7. Tape-out to Fab
8. Process Instabilities
PHTOLITHOGRAPHY

Basic Concept
Photolithography using positive photoresist
PHOTOLITHOGRAPHY

Photolithography using negative photoresist
OXIDATION

Oxidation of the silicon surface
OXIDATION

Oxidation through a window in the oxide
OXIDATION

Selective SiO$_2$ growth using local oxidation
Deposition of a thin solid layer

Non-uniformity $\Rightarrow$ Reliability problems
LAYER DEPOSITION

Thin layer of material in three different crystallographic forms deposited on single-crystal silicon
LAYERS DEPOSITION

Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD)
Epitaxy is a special case of CVD where a single-crystal silicon layer is deposited on a single-crystal silicon substrate.
Etching is the removal of material from areas unprotected by photoresist.

Wet Etching
An isotropic process using liquid chemicals.
ETCHING

Dry Etching
Using gas under reduced pressure.
Anisotropic
The processing step to introduce dopants into the semiconductor substrate.
Diffusion of dopants through a window in the SiO$_2$ layer.
DIFFUSION

Diffusion with constant source concentration.
DIFFUSION

Two step diffusion.

a) **Predeposition**: constant source concentration diffusion.

b) **Drive-in**: further diffusion without dopant source.
Ion implantation of dopants through a window in the SiO₂ layer.

To remove the damage created in the crystal lattice by the ion implantation, the wafer has to be annealed at a proper temperature and time period.
Effects of process variables in ion implantation.
LAYOUT TO FAB

IC Design.

Layout of an nMOS inverter.
Photolithographic Masks.

Design mask transformation.
LAYOUT TO FAB

IC Manufacturing Process.

Manufacturing wafer.
Errors in the location of the diffusion region boundary.
PROCESS INSTABILITIES

Mask misalignment.
PROCESS INSTABILITIES

Variations of the oxide thickness among and within IC chips at different locations of the wafer.
PROCESS INSTABILITIES

Process-Design Relationship.

Discrepancies between concepts used in the design and the actual elements of the IC: a) metal line, b) contact cut and c) diffusion region.
PROCESS INSTABILITIES

Geometrical Design Rules.

The minimal spacing between edges of two regions is determined by the fluctuations in the location of their boundaries in the actual IC.
A set of geometrical design rules for the nMOS technology, where $\lambda$ represents a unit spacing.