CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

Overview

1. Scan testing: design and application
2. At speed testing
3. The scan-set design technique
4. Scan testing power issues
5. The scan-hold design technique
6. Level sensitive scan design
7. Broadcast and Illinois scan design
Sequential Circuits Testing

In sequential circuits the initial state (register’s values) is not by default known. Consequently, the sensitization of faults and the propagation of the corresponding erroneous responses may turn to be a hard task.

A solution is to use techniques for the proper initialization of the circuit state to known values.

- Application of proper test vector sequences and/or the use of Set/Reset signals to setup the required state.
- Development of efficient techniques to set the initial state and observe the subsequent state after the response of the circuit.

General Scan Testing Scheme

The memory elements (latches or Flip-Flops) in a design are properly connected to form a unified shift register (scan register or chain). This way the internal state of the circuit is determined (controlled) by shifting in (scan-in) to the scan register the required test data to be applied to the combinational logic. Moreover, the existing internal state (previous logic response) can be observed by shifting out (scan-out) the data stored into the scan register.
Scan Testing Design (I)

Original Circuit

Scan Testing Design (II)

Multiple Scan Chains

Partial Scan

Combinational Logic

Register

PI PO

Primary Inputs

Primary Outputs

Scan-In

Pseudo-Primary Inputs

Scan-Out

Scan-In_1

Scan-In_N

Scan-Out_1

Scan-Out_N

Combinational Logic

Register

PI PO

PI PO

PI PO

Scan Register

Scan Register

Scan Register

Scan Register

Scan Register

Combinational Logic

Combinational Logic

Combinational Logic

Combinational Logic

Primary Inputs

Primary Outputs

Scan-In

Pseudo-Primary Inputs

Scan-Out

Scan-In

Scan-Out
Scan Path Design (I)

Scan Mode
SE="1"

Scan Testing

Scan Path Design (II)

Normal Mode
SE="0"

Scan Testing
Test Sequences During Scan Testing

Scan Application (I)

1. Scan cells testing

2. SE = “1”

3. Scan-in of alternating “0” and “1” from the SI input ≥ M+1 clock cycles

4. Response observation at the SO output

M = # of scan cells
Scan Application (II)

5. Logic testing

6. \( SE = "1" \): Test data scan-in from the SI inputs

\( M \) clock cycles (scan-in cycles)

7. \( SE = "0" \): Test pattern application from the PI inputs

8. Single clock pulse and response observation at the POs

\( single \) clock cycle (capture cycle)

Scan Testing

Scan Application (III)

9. \( SE = "1" \): New test data scan-in from the SIs and simultaneous scan-out of the test responses from the SOs

\( M \) clock cycles

10. Exists another test vector;

YES

7

NO

11. End

Scan Testing
Delay Fault Testing

A path delay fault requires a pair of subsequent test vectors to be detected. The first test vector initializes the circuit while the second test vector activates the path under test.

How can scan testing facilities be exploited for delay fault testing?

At speed clocking!

At Speed Scan Testing (I)
(Skewed-load or Launch-on-shift Technique)

Delay fault oriented scan testing technique
At Speed Scan Testing (II)
(Double Capture or Launch-on-Capture Technique)

Delay fault oriented scan testing technique

Fast Clock Pulses Generation

The Clocked-Scan Technique

The Scan-Set Technique (I)
The Scan-Set Technique (II)

Combinational Logic

The Scan-Set Technique (III)

Combinational Logic
The Scan-Set Technique (IV)

Combinational Logic

\[ X_1 \rightarrow Z_1 \]
\[ X_2 \rightarrow Z_2 \]
\[ \ldots \]
\[ X_n \rightarrow Z_n \]

PI \rightarrow PO

SE1 \(=0\)  SE2 \(=1\)

SCLK

Test Response Scan-Out SE1\(=0\) - SE2\(=1\)

Dual Flip-Flops Scan Architecture

Scan FF

Flip-Flop

D1 Master Latch
C1 D2
C2

Slave Latch

C

D

Q

System FF

D1 Slave Latch
C1 D2
C2

Master Latch

C

D

Q

from scan FF

from logic

SCB  SI  SCA

CUPTURE

UPDATE

to scan FF

to logic

Intel
Scan Testing Impact

- Silicon area and pin count cost.
- Speed performance degradation.
- Test application time cost.
- Excess power consumption (usually outside circuit’s specifications) during the scan-in/out operations and the capture of the test response in the scan chain.

Scan Chain Shift Power Consumption (I)

<table>
<thead>
<tr>
<th>Test Vector</th>
<th>Scan Chain</th>
<th>Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capture</td>
<td>0 1 1 0 1 0</td>
<td></td>
</tr>
<tr>
<td>Cycle 1</td>
<td>0 1 1 0 1</td>
<td>0</td>
</tr>
<tr>
<td>Cycle 2</td>
<td>0 1 1 0</td>
<td>1 0</td>
</tr>
<tr>
<td>Cycle 3</td>
<td>0 1 1</td>
<td>0 1 0</td>
</tr>
<tr>
<td>Cycle 4</td>
<td>0 1</td>
<td>0 0 1 0</td>
</tr>
<tr>
<td>Cycle 5</td>
<td>0</td>
<td>0 0 0 1 0</td>
</tr>
<tr>
<td>Cycle 6</td>
<td>0 1 1 0 1 0</td>
<td>1 0 0 0 1 0</td>
</tr>
</tbody>
</table>
Scan Chain Shift Power Consumption (II)

Test Vector  | Scan Chain  | Response
----------|-------------|--------
0 1 1 0 1 0 | 1 0 0 0 1 0 | 0
0 1 1 0 1   | 0 1 0 0 1   | 0 1 0
0 1 1 0     | 1 0 1 0 0   | 1 0
0 1 1       | 0 1 0 1 0   | 0 0 1 0
0 1         | 1 0 1 0 1   | 0 0 0 1 0
0           | 1 1 0 1 0   | 1 0 0 0 1 0

# Transitions = Distance from 1st scan-out bit

L = Scan chain length

Scan Chain Capture Power Consumption

Previous Test Vector 0 1 1 0 0
Previous Scan Chain State 0 1 1 0 1
Scan Chain 1 0 1 0 0
New Response 1 0 1 0 0
New Scan Chain State 1 0 1 0 0

Power consumption during scan testing procedures is a major concern since it can be several times higher than this during the normal mode of operation. This can affect the reliability of the circuit under test (CUT) due to overheating and electromigration phenomena. The excessive switching activity of the CUT during the scan operations may violate the power supply IR and LdI/dt drop limitations and increase the probability of noise induced test failures. In addition, the elevated temperature can degrade the speed performance of the CUT and result in erroneous test responses that will invalidate the testing process and lead to yield loss.
X-bit Assignment

• A large number of bits in a test cube that is generated by an ATPG tool are don’t care bits (X-bits).

• In order to apply a test cube for circuit testing, specific values must be assigned to the X-bits (test vector formation). This task is called X-filling.

• The X-filling process can be oriented for shift and/or capture power reduction.

Low Power Scan

Use of Data Gating (φραγμός δεδομένων) techniques at the output of the scan cells in order to eliminate the signal transitions at the inputs of the combinational logic during the scan-in/out operations. Dynamic power reduction.
Scan-Hold Flip-Flop

from logic

<table>
<thead>
<tr>
<th>Scan FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
</tr>
<tr>
<td>DI</td>
</tr>
<tr>
<td>SI</td>
</tr>
<tr>
<td>SE</td>
</tr>
<tr>
<td>CLK</td>
</tr>
</tbody>
</table>

to logic

Original Topology

from scan FF

Delay testing oriented Flip-Flop!
+ Dynamic power reduction.

to scan FF

The Scan-Hold Technique

<table>
<thead>
<tr>
<th>PI</th>
</tr>
</thead>
<tbody>
<tr>
<td>X_1</td>
</tr>
<tr>
<td>X_2</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>X_n</td>
</tr>
<tr>
<td>...</td>
</tr>
</tbody>
</table>

Combinational Logic

<table>
<thead>
<tr>
<th>D Scan FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>D Scan FF</td>
</tr>
<tr>
<td>D Scan FF</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>D Scan FF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SI</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
</tr>
<tr>
<td>Q</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>Latch</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>SE</td>
</tr>
<tr>
<td>Hold</td>
</tr>
<tr>
<td>Scan FF</td>
</tr>
</tbody>
</table>

to scan FF

Scan Testing
Level Sensitive Scan Design (I)

Level Sensitive Scan Design (II)

LSSD Design
IBM

Scan Testing
**Level Sensitive Scan Design (III)**

- **D-Latch and D-Flip-Flop Operation**

- **Non Overlapping Clocks**

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**Test Data Compression**

Typically, ATPG tools generate test vectors where only 1% to 5% of the bits have specified values!

On the other hand, test data volume is a major concern for the available bandwidth and the ATEs’ storage capabilities.
Linear Decompression

\[
\begin{align*}
Z_4 &= X_1 \oplus X_2 \oplus X_3 \\
Z_5 &= X_1 \oplus X_4 \oplus X_5 \\
Z_6 &= X_2 \oplus X_8 \oplus X_9 \\
Z_7 &= X_3 \oplus X_6 \oplus X_7 \\
Z_8 &= X_4 \oplus X_7 \oplus X_8 \\
Z_9 &= X_5 \oplus X_9 \oplus X_{10} \\
Z_{10} &= X_6 \oplus X_{12} \oplus X_{13} \\
Z_{11} &= X_7 \oplus X_{14} \oplus X_{15} \\
Z_{12} &= X_8 \oplus X_{16} \oplus X_{17} \\
Z_{13} &= X_9 \oplus X_{18} \oplus X_{19} \\
Z_{14} &= X_{10} \oplus X_{20} \oplus X_{21} \\
Z_{15} &= X_{11} \oplus X_{22} \oplus X_{23} \\
Z_{16} &= X_{12} \oplus X_{24} \oplus X_{25} \\
\end{align*}
\]

Broadcast & Illinois Scan Design

Broadcast Scan Design

Illinois Scan Design
Random–Access Scan Design

Combinational Logic

Row (X) Decoder

Column (Y) Decoder

Address Shift Register

Scan Cell

Reordering of Scan Chain Flip-Flops (I)

Typical Scan Chain

50 TV $\leq$ 300TV

Test Application: $300(20+1)+20 = 6320$ clock cycles

1st Alternative Test Application: $300(14+1)+8 = 4508$ clock cycles

"Random" register connection

Improvement 29%
Reordering of Scan Chain Flip-Flops (II)

2nd Alternative Scan Testing Application

\[
\text{Test Application: } 50(14+1) = 750 \text{ clock cycles} \\
250(12+1)+8 = 3258 \text{ clock cycles} \\
4008 \text{ clock cycles}
\]

Improvement 37% !

Reordering of Scan Chain Flip-Flops (III)

3rd Alternative Scan Testing Application with cell reordering

\[
\text{Test Application: } 50(18+1) = 950 \text{ clock cycles} \\
250(4+1)+4 = 1254 \text{ clock cycles} \\
2204 \text{ clock cycles}
\]

Improvement 63% !

In addition, test power reduction is achieved!
References