CMOS INTEGRATED CIRCUIT DESIGN TECHNIQUES

CMOS Logic Design

Survey on CMOS Digital Circuits

Dept. of Computer Science and Engineering

Y. Tsiatouhas

CMOS Integrated Circuit Design Techniques

Overview

1. Combinational – sequential logic
2. MOS transistor
3. CMOS logic
4. Complex gates
5. Standard cells

VLSI Systems and Computer Architecture Lab
Combinational and Sequential Logic

**Combinational Logic**

```
_outputs = f(inputs)
```

**Sequential Logic**

```
_outputs = f(inputs, state)
```

---

**Boolean Algebra**

**Axioms and Theorems**

<table>
<thead>
<tr>
<th>Equation</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>( x + 0 = x )</td>
<td>( x \cdot 1 = x )</td>
</tr>
<tr>
<td>( x + x = 1 )</td>
<td>( x \cdot x = 0 )</td>
</tr>
<tr>
<td>( x + x = x )</td>
<td>( x \cdot x = x )</td>
</tr>
<tr>
<td>( x + 1 = 1 )</td>
<td>( x \cdot 0 = 0 )</td>
</tr>
<tr>
<td>( x = x )</td>
<td></td>
</tr>
</tbody>
</table>

**Permutation prop.:**

\( x + y = y + x \)

\( x \cdot y = y \cdot x \)

**Associative prop.:**

\( x + (y + z) = (x + y) + z \)

\( x \cdot (y \cdot z) = (x \cdot y) \cdot z \)

**Distributive prop.:**

\( x(y + z) = xy + xz \)

\( x + (y \cdot z) = (x + y) \cdot (x + z) \)

**De Morgan:**

\( x + y = \overline{x} \cdot \overline{y} \)

\( x \cdot y = \overline{x + y} \)

\( x + xy = x \)

\( x \cdot (x + y) = x \)
Logic Gates

AND
\[ F = x \land y \]
\[
\begin{array}{c|c|c|c|c}
  x & y & F \\
  0 & 0 & 0 \\
  0 & 1 & 0 \\
  1 & 0 & 0 \\
  1 & 1 & 1 \\
\end{array}
\]

NAND
\[ F = \overline{x \land y} \]
\[
\begin{array}{c|c|c|c|c}
  x & y & F \\
  0 & 0 & 1 \\
  0 & 1 & 1 \\
  1 & 0 & 1 \\
  1 & 1 & 0 \\
\end{array}
\]

OR
\[ F = x \lor y \]
\[
\begin{array}{c|c|c|c|c}
  x & y & F \\
  0 & 0 & 0 \\
  0 & 1 & 1 \\
  1 & 0 & 1 \\
  1 & 1 & 1 \\
\end{array}
\]

NOR
\[ F = \overline{x \lor y} \]
\[
\begin{array}{c|c|c|c|c}
  x & y & F \\
  0 & 0 & 1 \\
  0 & 1 & 0 \\
  1 & 0 & 1 \\
  1 & 1 & 0 \\
\end{array}
\]

NOT
\[ F = \overline{x} \]
\[
\begin{array}{c|c|c}
  x & F \\
  0 & 1 \\
  1 & 0 \\
\end{array}
\]

XOR
\[ F = x \oplus y \]
\[
\begin{array}{c|c|c|c|c}
  x & y & F \\
  0 & 0 & 0 \\
  0 & 1 & 1 \\
  1 & 0 & 1 \\
  1 & 1 & 0 \\
\end{array}
\]

XNOR
\[ F = x \oplus y \]
\[
\begin{array}{c|c|c|c|c}
  x & y & F \\
  0 & 0 & 1 \\
  0 & 1 & 0 \\
  1 & 0 & 1 \\
  1 & 1 & 0 \\
\end{array}
\]

BUFFER
\[ F = x \]
\[
\begin{array}{c|c|c}
  x & F \\
  0 & 0 \\
  1 & 1 \\
\end{array}
\]

MOS Transistor

pMOS transistor
\[
\begin{array}{c}
  S \\
  G \\
  D \\
\end{array}
\]

nMOS transistor
\[
\begin{array}{c}
  G \\
  D \\
  S \\
\end{array}
\]

n-type semiconductor substrate

p-type semiconductor substrate
The MOS Transistor as Switch

\[ \begin{align*}
  s & \quad d \\
  g &= 0 \\
  s & \quad d \\
  g &= 1
\end{align*} \]

\[ \begin{align*}
  s & \quad d \\
  g &= 0 \\
  s & \quad d \\
  g &= 1
\end{align*} \]

The Full CMOS Switch

\[ \begin{align*}
  s & \quad d \\
  c &= 0 \\
  s & \quad d \\
  c &= 1
\end{align*} \]

\[ \begin{align*}
  s & \quad d \\
  c &= 0 \\
  s & \quad d \\
  c &= 1
\end{align*} \]
The Impact of Threshold Voltage

CMOS Logic

Inverter – NOT Gate
The P-network and N-network are complementary logic networks.

Static CMOS Circuits

- Each time (except input transition intervals) the output of a static CMOS gate is always attached either to the $V_{DD}$ power supply or the Gnd power supply. When a CMOS circuit is in the quiescent state, it is prohibitive for the two power supplies $V_{DD}$ and Gnd to be connected (in a short circuit).

- The connection of the output to the $V_{DD}$ power supply is through the pMOS network while the connection of the output to the Gnd power supply is through the nMOS network. When these networks are in a conducting state, behave as a low resistance resistor. In the opposite case, their resistance is considered to be infinite.
NAND Gate

- Circuit diagram of a NAND gate with inputs A and B, and output F.
- Karnaugh Map for the NAND gate, showing the truth table.
- Multiple Inputs NAND circuit with inputs B, C, and X.

NOR Gate

- Circuit diagram of a NOR gate with inputs A and B, and output F.
- Karnaugh Map for the NOR gate, showing the truth table.
- Symbol for the NOR gate.

CMOS Logic Design
**AND and OR Gates**

\[ F_p = A \cdot B \]

\[ F_n = \overline{A} \cdot \overline{B} \]

\[ F = A + B \]

\[ F = \overline{A} \cdot \overline{B} \]

---

**Complex Gates**

Implementation of the function:

\[ F = ((A \cdot B) + (C \cdot D)) \]

**pMOS network**

**nMOS network**

\[ \overline{F} = ((A \cdot B) + (C \cdot D)) \]

\[ F = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D}) \]
**CMOS Pass Gate**

Symbols

- **nMOS**
  - Off: \( V_{in} = 0 \), \( V_{out} = Z \)
  - On: \( V_{in} = 1 \), \( V_{out} = 1 \)

<table>
<thead>
<tr>
<th>( C = '0' )</th>
<th>nMOS off</th>
<th>pMOS off</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{in} = 0 ), ( V_{out} = 2 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{in} = 1 ), ( V_{out} = 2 )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>( C = '1' )</th>
<th>nMOS on</th>
<th>pMOS on</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{in} = 0 ), ( V_{out} = 0 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{in} = 1 ), ( V_{out} = 1 )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Tri-State Inverter**

Truth Table

<table>
<thead>
<tr>
<th>( V_{in} )</th>
<th>( C )</th>
<th>( V_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>0</td>
<td>Z</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Symbol
**Multiplexer**

Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>S</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0 (B)</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>0</td>
<td>1 (B)</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>1</td>
<td>0 (A)</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>1</td>
<td>1 (A)</td>
</tr>
</tbody>
</table>

**Latch**

Truth Table

<table>
<thead>
<tr>
<th>D</th>
<th>CLK</th>
<th>Q</th>
<th>Qbar</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Memory</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Memory</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
D Flip-Flop

CMOS Edge Triggered D Flip-Flop

D Flip-Flop Operation

Positive Edge-Triggered D Flip-Flop

Truth Table

<table>
<thead>
<tr>
<th>D</th>
<th>CLK</th>
<th>Q</th>
<th>Qbar</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>0</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>Memory</td>
<td></td>
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