Novel TSC Checkers for Bose-Lin and Bose Codes

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Abstract

This paper presents a novel method for designing single and double output checkers for Bose-Lin and Bose codes. Bose-Lin codes are systematic t-unidirectional error detecting codes while Bose codes is a class of burst unidirectional error detecting codes. The proposed checkers are the first Totally Self Checking (TSC) checkers for Bose-Lin and Bose codes that take into account a realistic fault model including stuck-at, transistor stuck-open, transistor stuck-on and resistive bridging faults. Furthermore, the proposed checkers are very compact and fast. The single output TSC checkers proposed in this paper are the first single output checkers presented in the open literature, for Bose-Lin and Bose codes.

I. Introduction.

It is well known that the most common errors in VLSI circuits are unidirectional in nature [1-3]. The Berger code is an optimal systematic code that can detect all unidirectional errors [4]. However in many applications it is sufficient to detect up to t unidirectional errors. The value of t, of course, will depend on the bit organization, layout, etc. Some of the known systematic t-Unidirectional Error Detecting (t-UED) codes have been presented in [5-7]. In certain applications, such as semiconductor memory architectures, the unidirectional errors tend to occur in a burst, i.e., a cluster of adjacent bits up to a certain length is affected. Burst Unidirectional Error Detecting (BURD) codes have been proposed by Bose [8] and Blaum [9]. The Blaum code for a specific number r, r≥4, of check bits detects burst unidirectional errors with longer length than the codes given by Bose [8]. However encoding and decoding in the Blaum codes is significantly more complicated than in Bose codes. The suitability of a code for use in a computer system, apart from its ability to cope with errors, heavily depends on the existence of a simple and fast encoder and decoder [10].

A circuit consisting of a functional circuit, whose output words belong to a certain code, and a checker that monitors the output of the functional circuit and indicates if it is a code or a non-code word is called Self Checking Circuit (SCC) [11]. These circuits can provide concurrent error detection and thus can detect transient, intermittent as well as permanent faults. Since transient faults have become increasingly dominant in VLSI circuits [12-14], providing protection against them has become very important. The reliability of a SCC depends on the ability of its checker to behave correctly despite the possible occurrence of internal faults. It has been shown that this is achieved when the checker satisfies either the Totally Self Checking (TSC) [15] or the Strongly Code Disjoint (SCD) [16] property. In this paper we will take into account the TSC property. A circuit is a TSC checker if it is self-testing, fault-secure and code disjoint [15, 17].

TSC checkers for Bose-Lin t-UED codes [6] and Bose BUED codes [8] under the single stuck-at fault model were proposed in [18-20]. However, the conventional stuck-at fault model has been found to be inadequate for CMOS circuits [21]. CMOS is the current dominant technology for manufacturing VLSI circuits, thus new TSC checker designs are required that will take into account a more realistic fault model including apart from stuck-at, transistor stuck-open, transistor stuck-on and resistive bridging faults.

In this paper a new method for designing TSC checkers for t-UED Bose-Lin codes and BUED Bose codes is proposed. The checkers designed according to this method are TSC with respect to stuck-at, transistor stuck-on, transistor stuck-open and resistive bridging faults. The proposed checkers are significantly more efficient, with respect to area and speed, than the corresponding already known TSC checkers.

There are cases that a single output TSC checker with its output two rail encoded in time may have some advantages over the double output checker [26, 22]. No single output TSC checker for t-UED codes and BUED codes is up today known from the open literature. To this end, apart from double output we also present single output TSC checkers for t-UED Bose-Lin and BUED Bose codes.

Throughout this paper the following notations are used :

- k (r) number of information (check) bits.
- $I_1, I_2, \ldots I_k$ ($C_0, \ldots, C_{r-1}$) are the information (check) bits.
- $W^0(X)$ denotes the number of zeroes of the vector X.
- V_{OHMIN} (V_{OLMAX}) is the minimum HIGH (maximum LOW) voltage at the output of a circuit.
- V_{tn} (V_{tp}) is the threshold voltage of n (p) transistor.
- KP_n (KP_p) is the Spice parameter for $\mu_n C_{ox}$ ($\mu_p C_{ox}$).
- W_{qi}/L_{qi} (W_{pi}/L_{pi}) is the ratio of n (p) transistor i.

II. Preliminaries

A. *The Bose BUED Codes.*

This code can detect a burst unidirectional error in up to 2^{r-1} bits. The check symbol CS is obtained as $CS = W^0(I_1, \ldots, I_k) \bmod 2^r$ and the bits of the code word are arranged as follows: $I_1 I_2 \ldots I_{k-2^{r-1}} C_{r-1} I_{k-2^{r-1}+1} \ldots I_{k-1} I_k C_{r-2} C_{r-3} \ldots C_0$.

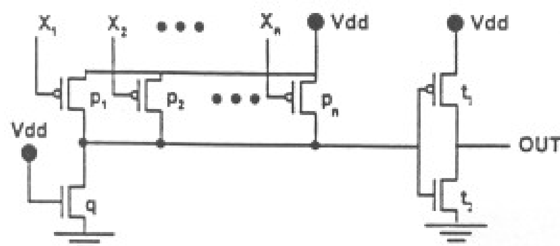

Figure 1. m-zeroes threshold circuit

B. *The Bose-Lin t-UED Codes.*

Bose and Lin gave optimal t-UED codes with t=2, 3 and 6 using 2, 3 and 4 bits respectively. The check symbol CS for these codes is derived as follows:

i. 2-UED code with r=2 : $CS = W^0(I_1, \ldots, I_k) \bmod 4$,

ii. 3-UED code with r=3 : $CS = W^0(I_1, \ldots, I_k) \bmod 8$,

iii. 6-UED code with r=4 : $CS = (W^0(I_1, \ldots, I_k) \bmod 8) + 4$ or equivalently $CS=C_3C_2C_1C_0$ where $C_3=D_2$ $C_2=\overline{D_2}$ $C_1=D_1$ $C_0=D_0$ and $D_2D_1D_0 = W^0(I_1, \ldots, I_k) \bmod 8$.

iv. For $r \geq 5$ Bose-Lin have given two methods for designing t-UED codes. For $r \geq 6$ the codes designed following the second method detect more unidirectional errors. However, the encoder and decoder of the codes designed by the first method is simpler and faster than the codes designed by the second method. According to the first method the check symbol is given as $CS = (W^0(I_1, \ldots, I_k) \bmod 2^{r-1}) + 2^{r-2}$ or equivalently $CS=C_{r-1}C_{r-2}C_{r-3}\ldots C_0$ where $C_{r-1}=D_{r-2}$, $C_{r-2}=\overline{D_{r-2}}$, $C_{r-3}=D_{r-3}$, ..., $C_0=D_0$ and $D_{r-2}D_{r-3}\ldots D_0$ is the binary representation of $W^0(I_1, \ldots, I_k) \bmod 2^{r-1}$. This code can detect up to $2^{r-2}+r-2$ unidirectional errors.

III. Design Method

A. *Threshold circuits*

Definition 1. A circuit with n inputs, $X_1, \ldots, X_n$ and one output, OUT, is called m-zeroes threshold circuit, if : when $W^0(X_1, \ldots, X_n) \geq m$ then OUT is Low else OUT is High.

Following the same design procedure as in [23] we can see that the circuit of figure 1 is an m-zeroes threshold circuit if the following relations are satisfied:

a. $W_{P_1}/L_{P_1} = W_{P_2}/L_{P_2} = \cdots = W_{P_n}/L_{P_n} = (W/L)_p$

b. $(m-1)\cdot 1/Q_2 \cdot (W/L)_p \leq W_q/L_q \leq m\cdot 1/Q_1 \cdot (W/L)_p$ (1)

where $Q_1 = KP_n/KP_p \cdot \left(2(V_{dd}-V_{tn})V_{OHMIN} - V^2_{OHMIN}\right)/\left(V_{dd}+V_{tp}\right)^2$,

$Q_2 = KP_n/KP_p \cdot \left(2(V_{dd}-V_{tn})V_{OLMAX} - V^2_{OLMAX}\right)/\left(V_{dd}+V_{tp}\right)^2$

The zeroes-weight, $TW^0(C)$, of an m-zeroes threshold circuit is by definition equal to m.

Definition 2. A circuit C with n+z inputs $X_1, \ldots, X_n$ and $Y_1, \ldots, Y_z$ and one output OUT is called a $(V_1, \ldots, V_z)$ aggregate-zeroes threshold circuit with $V_1, \ldots, V_z \in N^*$ if for each vector $Y_1, \ldots, Y_z$ the circuit operates as follows: when $W^0(X_1, \ldots, X_n) \geq Y_1V_1 + \cdots + Y_zV_z$ then OUT is Low else OUT is High.

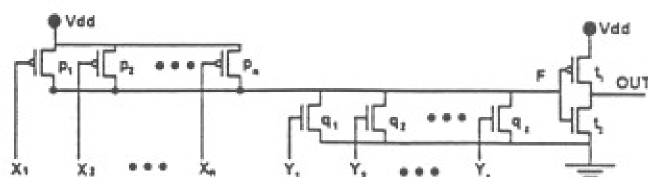

Figure 2. $(V_1, \ldots, V_z)$ aggregate-zeroes threshold circuit

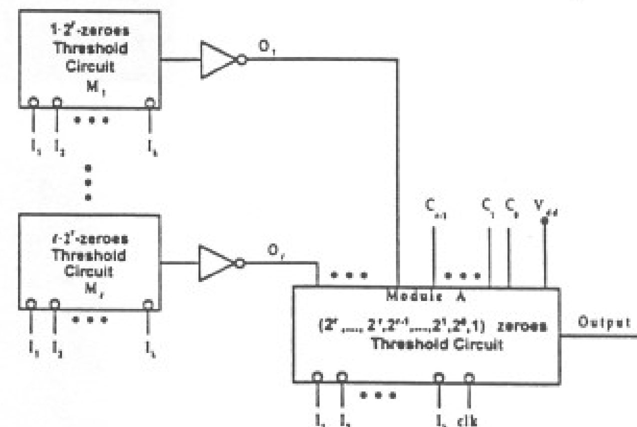

Figure 3. Single Output BUED Bose code checker.

The sum $Y_1V_1 + \cdots + Y_zV_z$ is called the aggregate-zeroes-weight, $AW^0_C(V, Y)$ of the circuit for the vector $Y_1, \ldots, Y_z$. The circuit of Figure 2 is an $(V_1, \ldots, V_z)$ aggregate-zeroes threshold circuit, if the following relations are satisfied:

a. $W_{P_1}/L_{P_1} = W_{P_2}/L_{P_2} = \cdots = W_{P_n}/L_{P_n} = (W/L)_p$

b. $(V_i - 1/z)\cdot 1/Q_2 \cdot (W/L)_p \leq W_{q_i}/L_{q_i} \leq V_i \cdot 1/Q_1 \cdot (W/L)_p$ $i \in [1, z]$ (2)

B. *TSC Checkers for the Bose BUED codes.*

Consider the circuit of figure 3, where $\ell = \lfloor k/2^r \rfloor$. Based on the definitions of the threshold circuits we get:

$O_i = 1$ if $W^0(I_1, \ldots I_k) \geq i\cdot 2^r$ else $O_i = 0$ for $i \in [1, l]$

$AW^0_A(V,Y) = 2^rO_\ell + \cdots + 2^rO_1 + C_{r-1}2^{r-1} + \ldots + C_0 + 1$ where $Y=(O_1, \ldots, O_\ell, C_{r-1}, \ldots, C_1, 1)$ and $V=(2^r, \ldots, 2^r, 2^{r-1}, \ldots, 2^0, 1)$

Now we have that

$O_1 + \ldots + O_\ell = [W^0(I_1, \ldots, I_k)/2^r] = W^0(I_1, \ldots, I_k) - W^0(I_1, \ldots, I_k) \bmod 2^r$,

where [x] denotes the integral part of x. Therefore

$$AW^0_A(V,Y) =$$

$$W^0(I_1, \ldots, I_k) - W^0(I_1, \ldots, I_k) \bmod 2^r + 2^{r-1}C_{r-1} + \ldots + C_0 + 1 \quad (3)$$

Consider that the input clk is driven by the system clock, $I = (I_1, \ldots I_k)$ is the information part and $C = (C_0C_1\ldots C_{r-1})$ is the check symbol corresponding to I. In the following we will show that the circuit of figure 3 is a single output checker for the BUED Bose codes.

When $I_1I_2 \ldots I_k$, $C_{r-1}\ldots C_1C_0$ is a code word of the Bose BUED code then we have $CS=W^0(I_1, \ldots I_k) \bmod 2^r$ or equivalently $2^{r-1}C_{r-1} + \ldots + 2C_1 + C_0 = W^0(I_1, \ldots I_k) \bmod 2^r$. Then taking into account (3) we get

$$AW^0_A(V, Y) = W^0(I_1, \ldots I_k) + 1. \quad (4)$$

According to definition 2 we have that when

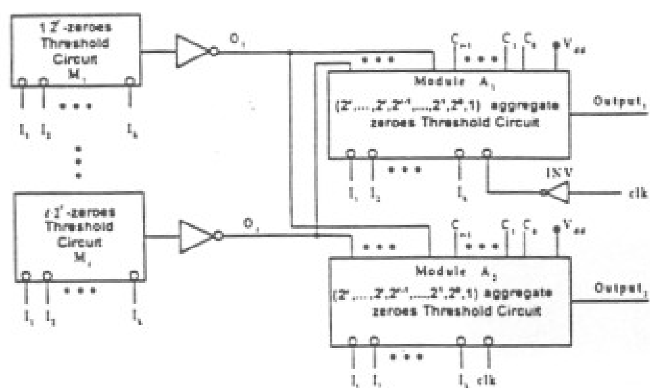

Figure 4. Double output BUED Bose code checker.

$W^0(I_1, \ldots I_k, clk) \geq AW_A^0(V, Y)$ then Output=0 else Output=1. For clk=1 we have $W^0(I_1, \ldots I_k, clk)=W^0(I_1, \ldots I_k)$, thus taking into account relation (4) we get $W^0(I_1, \ldots I_k, clk) < AW_A^0(V,Y)$ hence Output=1. For clk=0, $W^0(I_1, \ldots I_k, clk)=W^0(I_1, \ldots I_k)+1$ thus taking into account relation (4) we get
$W^0(I_1, \ldots I_k, clk) = AW_A^0(V, Y)$, hence Output=0.
When $I_1I_2 \ldots I_k, C_{r-1}, \ldots, C_1C_0$ is not a code word of the BUED Bose code we have that

$$CS \neq W^0(I_1, \ldots I_k) \bmod 2^r \text{ or equivalently}$$

$$2^{r-1}C_{r-1}+\ldots+2C_1+C_0=W^0(I_1, \ldots, I_k) \bmod 2^r + a, \quad 0<|a|<2^r,$$

thus taking into account relation (3) we get

$$AW_A^0(V, Y) = W^0(I_1, \ldots I_k)+a+1.$$

When a>0 then for either clk=0 or clk=1 we have
$AW_A^0(V, Y)>W^0(I_1, \ldots I_k, clk)$, therefore we get Output=1, while when a<0 then for either clk=0 or clk=1 we have
$AW_A^0(V, Y)<W^0(I_1, \ldots I_k, clk)$, therefore we get Output=0.

From the above it is obvious that when the input vector IC is a code word of the BUED Bose code and the circuit is fault free then during a period of the signal clk the output OUT gets the values (0, 1). When the input vector is not a code word, then during a period the output OUT gets the values (1, 1) or (0, 0). In other words the circuit of figure 3 is a single output BUED Bose code checker. As in the case of the single output comparator given in [22] the output of the checker can be simply checked using a flip flop. The flip flop is triggered by a clock signal identical to the system clock, but delayed with respect to system clock, by a suitably chosen time interval (taking into account the checker input/output delay and the flip flop setup time). The output of the checker is sampled on both the triggering signal rising and falling edges (as the flip flop presented in [24]).

From the above it is easy to see that the checker input/output delay, t_d, plus the flip flop setup time t_s, must be smaller than the half of the period of the system clock. This implies that the single-output TSC BUED Bose code checker can be used only in systems with period greater than $2(t_d+t_s)$ (the same comment concerns the single output comparators given in [22]). However as we will see the delay of the proposed single output checkers is very small, thus they can be used in most applications.

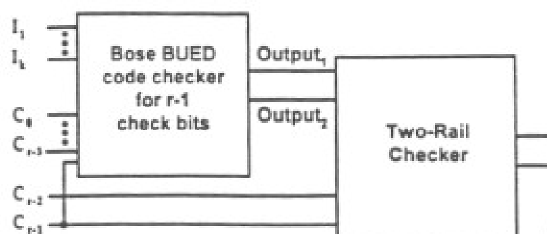

Figure 5. Double output Bose-Lin code checker for r≥4.

Figure 4 presents the double output checker for the Bose BUED code. In this checker, modules A_1, A_2 which are identical to module A of Figure 4 are driven by the signal clk and the inverted clk respectively. The input clk is driven by a clock signal with the half frequency of feeding inputs to the checker. This feeding frequency is usually equal to the frequency of the system clock, therefore the signal driving input clk can be easily obtained from the system clock using a T flip flop. So, when the checker receives a code word of the BUED Bose code, $(Output_1, Output_2) = (0, 1)$ for clk=1 and $(Output_1, Output_2) = (1, 0)$ for clk=0. When the received word is not a code word $(Output_1, Output_2)$ is either (0, 0) or (1, 1), thus it is not two-rail encoded.

The manufacturability of the proposed checkers depends on the manufacturability of the ratioed m-zeroes and aggregate-zeroes threshold circuits. A problem of a ratioed circuit is that its correct operation depends on the conductance values of nmos and pmos transistors as well as the other circuit parameter's values. It is well known that fluctuations in integrated circuit manufacturing processes cause deviations on the actual values of the parameters from their nominal values. Designing the m-zeroes and aggregate -zeroes threshold circuits we choose the values of W_p, and L_p so that the value of W_p/L_p to be in the middle of the ranges given by relations (1) and (2). Then due to statistical variations of the device characteristics the range can be shortened or shifted to the left or to the right but the value of W_p/L_p will remain within the range, therefore the manufactured IC will operate correctly. As the values of r and/or k (we remind that in figures 3, 4 $\ell = \lfloor k/2^r \rfloor$) become greater the range defined by relation (1) and (2) become shorter and the yield of the manufacturing process will become smaller. With the improvement of a manufacturing process the circuit parameters deviation becomes smaller and the m-zeroes threshold circuits as well as aggregate-zeroes threshold circuits for larger values of r and k can be constructed. However, given the quality of a manufacturing process there exist a maximum value of r and k for which BUED Bose code checkers can be constructed following our method. Taking into account that the value of k is much larger than the value of r, we conclude that the value of k specifies the limit.

C. TSC Checkers for the Bose-Lin codes.

It is evident that the single and double output TSC checkers given in figures 4, 5 are also TSC checkers for the

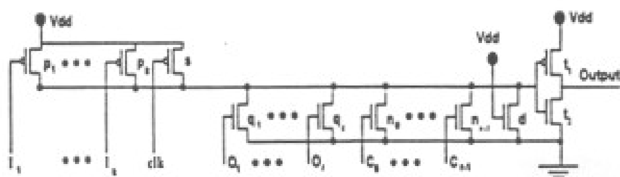

Figure 6. Module A.

Bose-Lin code with r=2, 3 check bits. The TSC checker for r≥4 is given in figure 5. The two-rail checker is designed as proposed in [25]. It is obvious that the circuit of figure 5 is a TSC checker for Bose-Line codes with $r \geq 4$.

IV. Testability Analysis.

All the inverters are designed with n-dominate logic.

Single output checker (figure 3). The notation $Output_{0,1}$= Q, R means that during a clock period, when clock is low, Output=Q and when it is high Output=R. We verified that all stuck-at, transistor stuck-open and stuck-on faults are detected by a single code word except of the following faults:

$2^r \cdot m$-Zeroes Threshold circuit $1 \leq m \leq \ell$ (Figure 1 for n=k).

1. Transistor q stuck-on or transistor t_2 stuck-on: Any one of these faults is not detected but after its occurrence the checker remains code disjoint. Furthermore if this fault is followed by one of the other considered faults, the resulting fault is detectable.
2. Transistor t_1 stuck-open: When the checker receives two successive code words, the first with $W^0(I_1,\ldots,I_k) \geq 2^r \cdot m$ and the second with $W^0(I_1,\ldots,I_k) < 2^r \cdot m$ then at the second code word $Output_{0,1}$ = 1, 1.
3. Transistor t_2 stuck-open : When the checker receives two successive code words, the first with $W^0(I_1,\ldots,I_k) < 2^r \cdot m$ and the second with $W^0(I_1,\ldots,I_k) \geq 2^r \cdot m$ then at the second code word $Output_{0,1}$ = 0, 0.

Module A. The circuit of this module is shown in Figure 6.

1. Transistor d stuck-on or transistor t_1 stuck-on : Any one of these faults is not detected but after its occurrence the checker remains code disjoint. Furthermore if this fault is followed by one of the other considered faults, the resulting fault is detectable.

The self-checking capability with respect to resistive bridging faults has been evaluated with extensive circuit-level simulations. Resistive bridging faults (RBFs) between two transistor terminals or between two inputs have been considered. All RBFs with connecting resistance $R \in [0, R_{max}]$ are detected, where R_{max} depends on the sizing of the transistors. We are interested for resistances in the range [0, 6KΩ] [27]. For the 8 bit BUED Bose code checker of figure 3 and an implementation in λ=1μm technology with transistor aspect ratios $(W/L)p_i$=6/1, (W/L)q=8/1 (M_1), (W/L)q=16/1 (M_2), $(W/L)q_1$=8/1, $(W/L)q_2$=8/1, $(W/L)n_0$=2/1, $(W/L)n_i$=4/1, (W/L)s=6/1, (W/L)d=2/1 the value of R_{max} is given in Table 1. The inputs of the checker

Table 1. Resistive Bridging Faults.

Bridging Fault	Maximum Resistance	Bridging Fault	Maximum Resistance
I_i - V_{dd}	5.25 kΩ	F_2 - Gnd	5.3 kΩ
I_i - F_1	6 kΩ	F - V_{dd}	5.75 kΩ
I_i - F_2	5.5 kΩ	F - Gnd	6 kΩ
I_i - F	6 kΩ	C_1 - Gnd	4 kΩ
I_i - I_{i+1}	undetectable	C_0 - Gnd	1.8 kΩ
O_4 - O_8	6 kΩ	clk - F	undetectable
O_4 - Gnd	6 kΩ	clk - V_{dd}	6 kΩ
O_4 - V_{dd}	2.65 kΩ	C_1 - V_{dd}	2.1 kΩ
O_8 - Gnd	5.75 kΩ	C_0 - V_{dd}	1.6 kΩ
O_8 - V_{dd}	2.65 kΩ	O_8 - C_1	5.3 kΩ
F_1 - V_{dd}	4.1 kΩ	C_1 - C_0	3 kΩ
F_1 - Gnd	6 kΩ	clk - Gnd	0.9 kΩ
F_2 - V_{dd}	6 kΩ	-	-

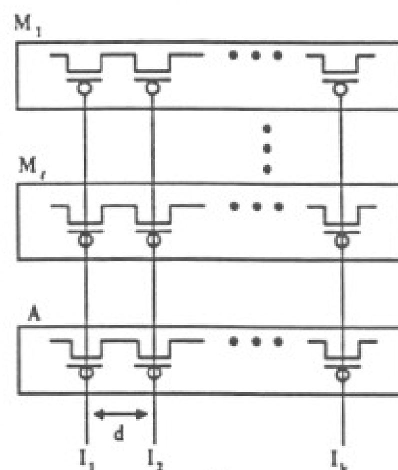

Figure 7. The physical place of transistors and input lines in this figure presents their place in lay-out level.

are driven by standard cell inverters with $(W/L)_p$=12 and $(W/L)_n$=6. The bridging fault between two input lines I_i and I_{i+1} is undetectable but the possibility of such a fault in our design is very small. Due to the proposed layout, figure 7, and the lay out rules of the used 1μ technology the distance d between two adjacent input lines is 5μ while the minimum distance between two lines in this technology is 2μ. Therefore, due to the relatively large distance between any pair of adjacent input lines I_i and I_{i+1}, the possibility of bridging faults is very small. If the checker receive the code words with a) I_i=1, $W^0(I_1,\ldots,I_k)=2^r m-1$ and b) I_i=0, $W^0(I_1,\ldots,I_k)=2^r m$ with $i \in [1, k]$, $m \in [1, \ell]$ and for every value of m a pair of code words I_1, I_2 with $W^0(I_1)=2^r m-1$, $W^0(I_2)=2^r m$ and a pair I'_1, I'_2 with $W^0(I'_1)=2^r m$ and $W^0(I'_2)=2^r m-1$ then all detectable faults will be detected.

Therefore the number of the necessary code words is equal to

$$TS=\sum_{m=1}^{\lfloor k/2^r \rfloor}\left(\left\lceil k/(k-2^r m+1)\right\rceil+\left\lceil k/2^r m\right\rceil\right)$$ among which $4\lfloor k/2^r \rfloor$

Table 2. Improvement of Proposed over Piestrak'[20]

(k, r)	Delay		Area	
	Single Output	Double Output	Single Output	Double Output
(8, 2)	-20%	37.6 %	88 %	83 %
(16, 2)	-14.6 %	41.3 %	87.4 %	84.5 %
(16, 3)	0 %	48.8 %	93.4 %	90.8 %

'The checkers proposed in [20] are double output checkers.

must be pairs of code words. For (k, r): (32, 2) (32, 3) (64, 4) the proposed checker require 54, 37 and 69 code words among which 8, 4 and 4 should be pairs of code words respectively. It is evident that the test set is very small.

The testability analysis of the double output checkers of figure 4 and 5 is similar to that of figure 3.

V. Comparisons and Conclusions.

In this paper we presented a novel method for designing single and double output TSC checkers for BUED Bose and t-UED Bose-Lin codes. The proposed checkers are the first known checkers for these codes, that are TSC under a realistic fault model including stuck-at, transistor stuck-on, transistor stuck-open and resistive bridging faults. The corresponding already known checkers [18-20] are TSC under the stuck-at fault model. The proposed single output TSC checkers for BUED Bose and t-UED Bose-Lin codes are the only known in the open literature.

Among the TSC checkers already proposed [18-20], the checkers given in [20] are the most efficient with respect to the area required for their implementation and the delay. To this end we compare our checkers to the checkers given in [20]. We have implemented some of the proposed TSC checkers as well as the corresponding checkers given in [20] with $\lambda=1\mu m$ technology. The comparison results are given in Table 2. The area has been estimated as the sum of WxL of the transistors, that is, the routing has not been taken into account. We can see that the routing in the proposed design is less than the routing of the checkers given in [20]. It is also obvious that the proposed single and double output checkers are impressively more efficient, with respect to the area, than checkers given in [20], while the proposed double output checkers are also significantly faster.

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